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MS-7D20

mATX
Ver: 10

RKL Platform

CPU:

Comet lake S 35W

Onboard Chip:

HD Audio Codec : ALC897

LAN : RTL8125B-CG COLAY RT8111K

SIO : NTC6687

Flash ROM: SPI 256 MB X1

Main Memory:

*DDRIV (2666MHz) * 2*

PWM:

IMVP8 -NCP81267

ACPI:

LDO

Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X1) Slot * 2*

*M.2 Slot * 1*

System Chipset:

B560 PCH_V

VGA Output:

HDMI Port

DVI Port

VGA Port

Other:

*SATA3.0 *6*

*PS2 * 1*

*REAL USB3.1 *2*

REAL USB3.0 LAN_USB

*FRONT USB3.1 *2*

*FRONT USB2.0 *4*

MICRO-STAR INT'L CO.,LTD			
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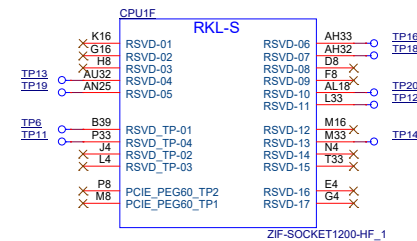


Diagram illustrating the pin connections for the ZIF-SOCKET1200-HF 1. The diagram shows two columns of pins, each with 1200 pins, connected to various DMI signals.

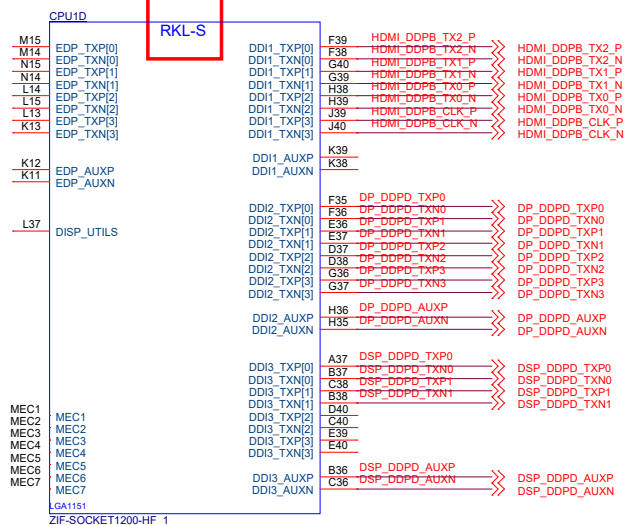
Left Column (Pins 1-1200):

- DMI_RXP0 (Pin 1)
- DMI_RXN0 (Pin 2)
- DMI_RXP1 (Pin 3)
- DMI_RXN1 (Pin 4)
- DMI_RXP2 (Pin 5)
- DMI_RXN2 (Pin 6)
- DMI_RXP3 (Pin 7)
- DMI_RXN3 (Pin 8)
- DMI_RXN7 (Pin 1200)

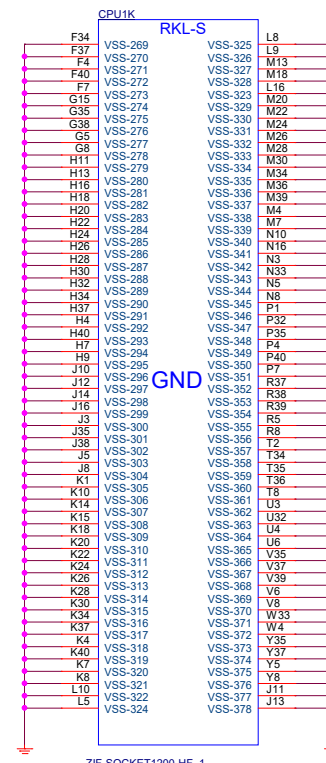
Right Column (Pins 1201-2400):

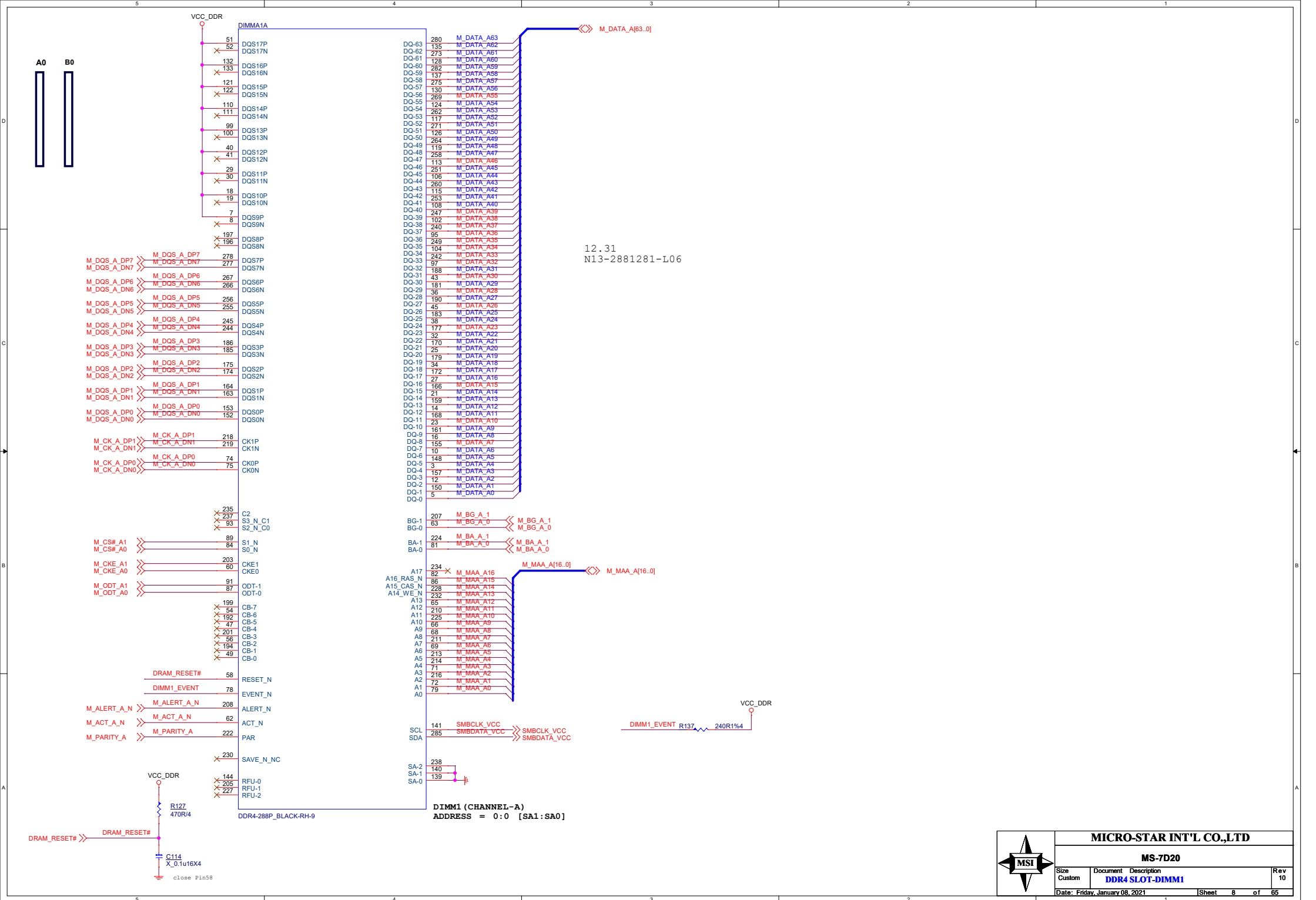
- DMI_TXP0 (Pin 1201)
- DMI_TXN0 (Pin 1202)
- DMI_TXP1 (Pin 1203)
- DMI_TXN1 (Pin 1204)
- DMI_TXP2 (Pin 1205)
- DMI_TXN2 (Pin 1206)
- DMI_TXP3 (Pin 1207)
- DMI_TXN3 (Pin 1208)
- DMI_TXN7 (Pin 2400)

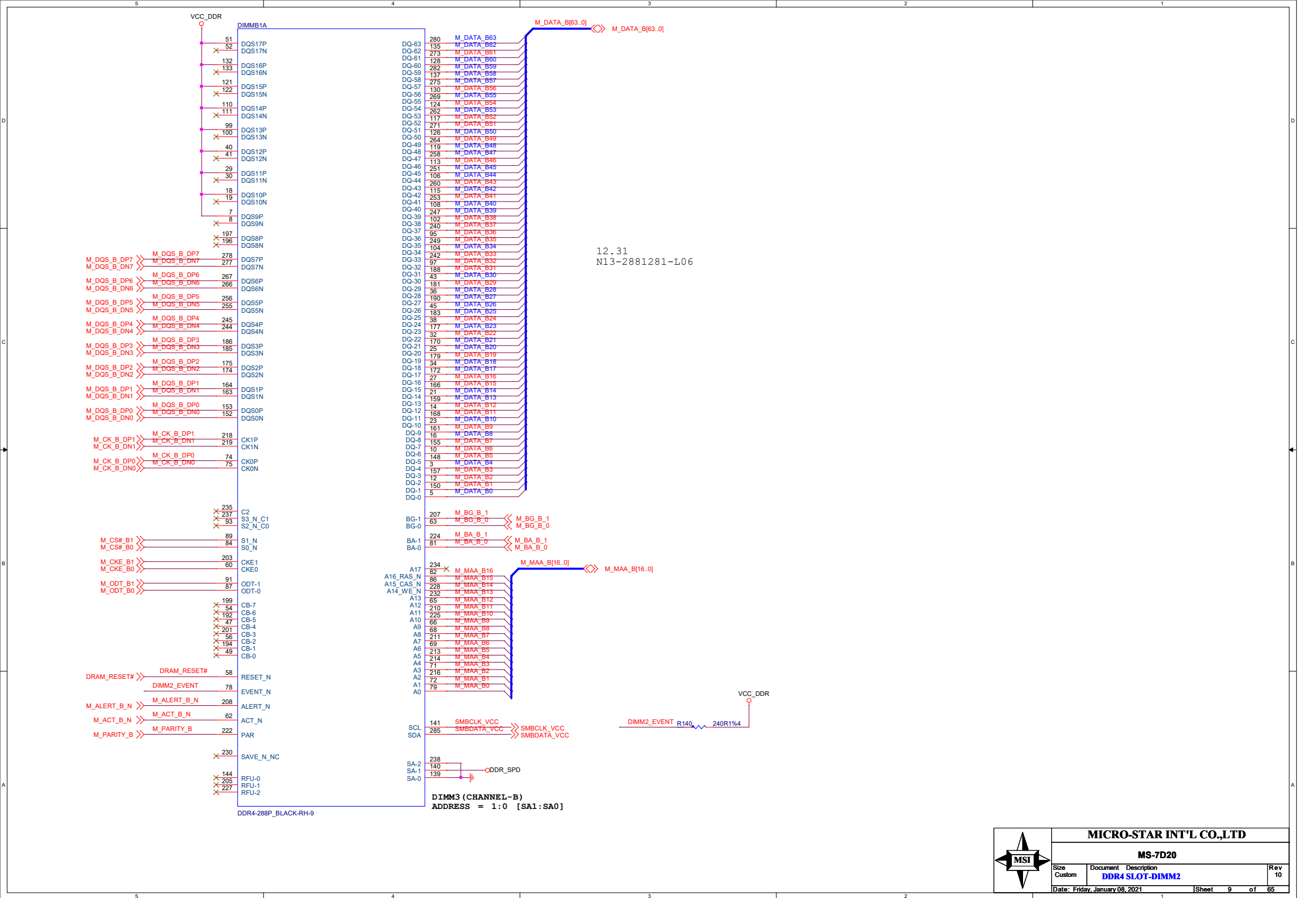
The diagram shows that the pins are connected to the DMI signals in a specific pattern, with the left column connected to RX signals and the right column connected to TX signals.

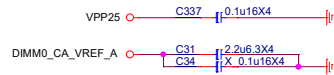
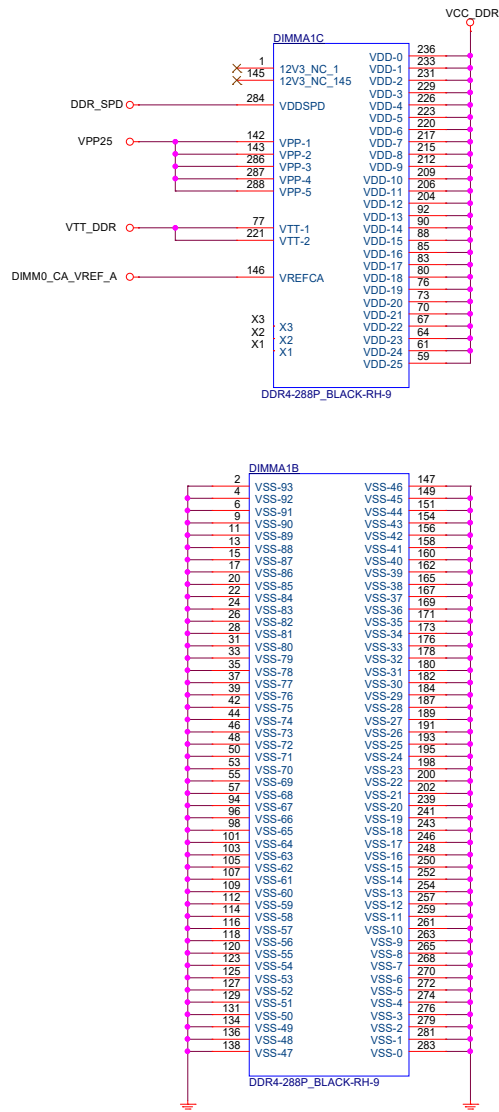


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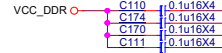
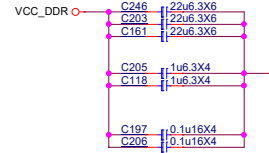
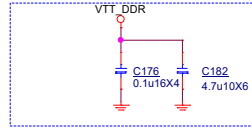




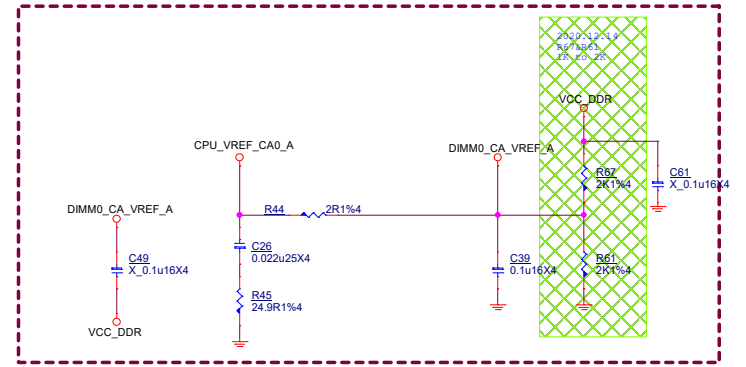
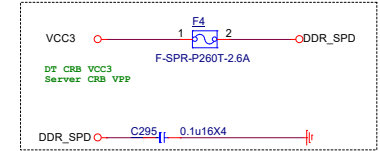




0.1uFx1 per dimm



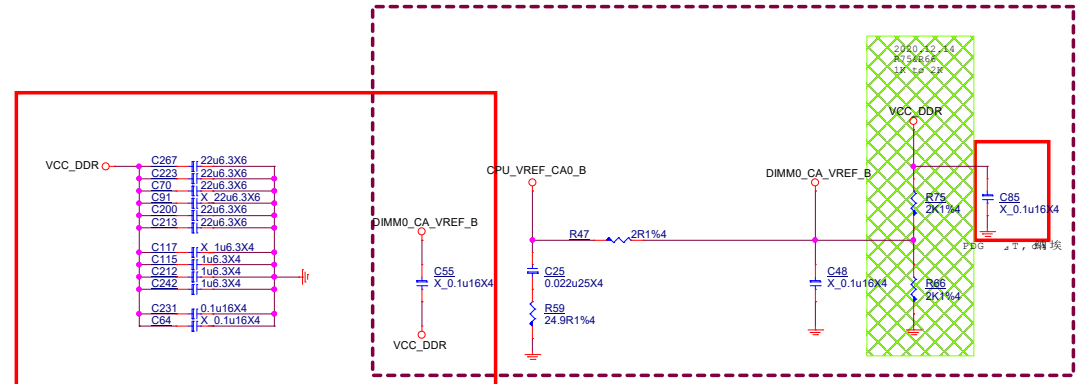
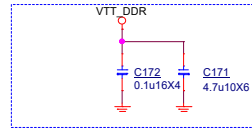
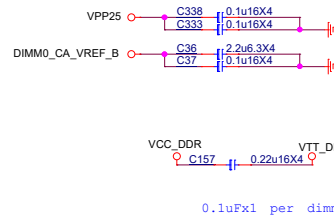
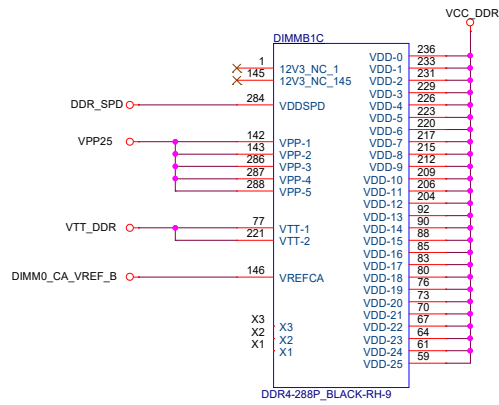
MLCC for VCC_DDR



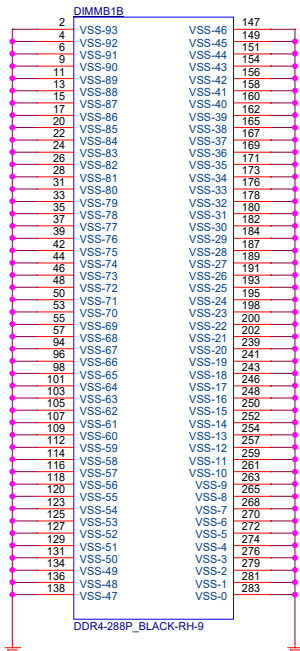
MICRO-STAR INT'L CO.,LTD

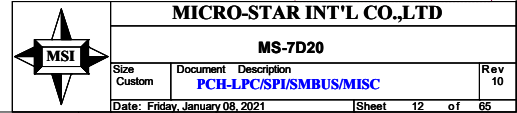
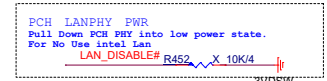
MS-7D20

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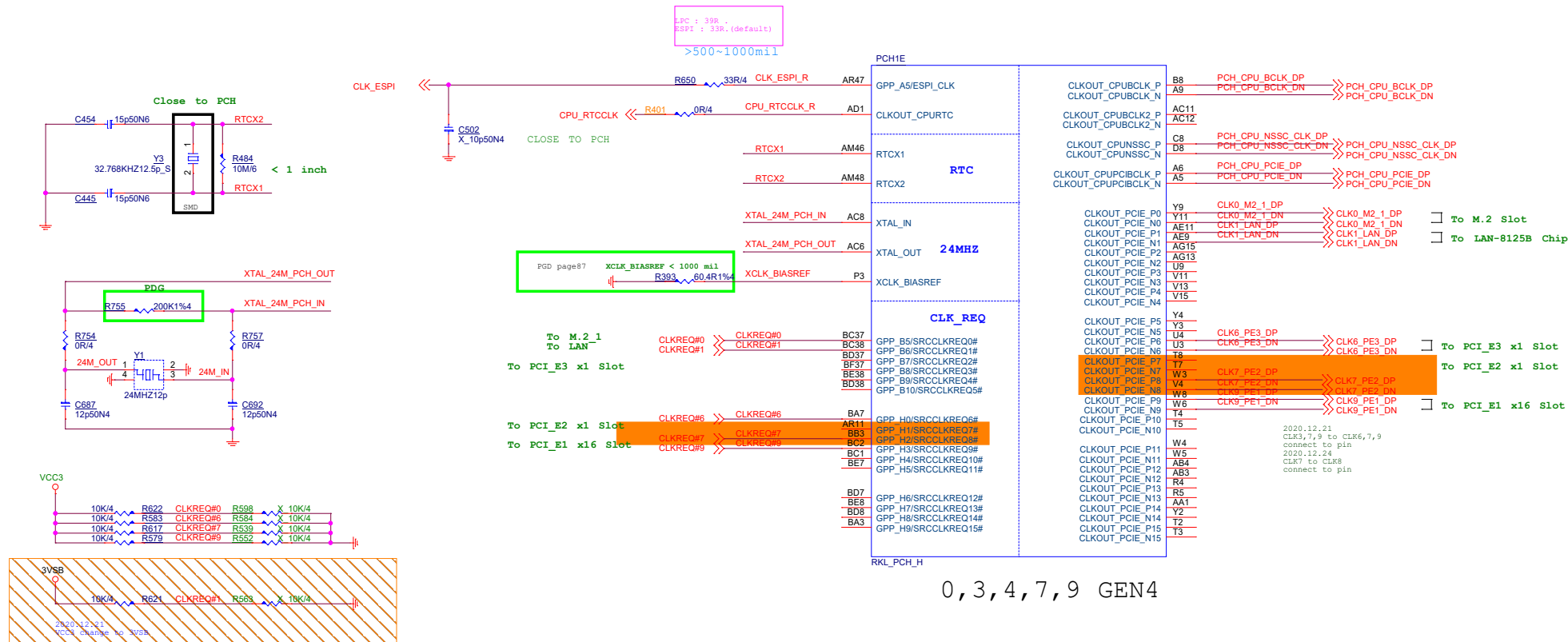


7D20 STUFF CAP COUNT ?

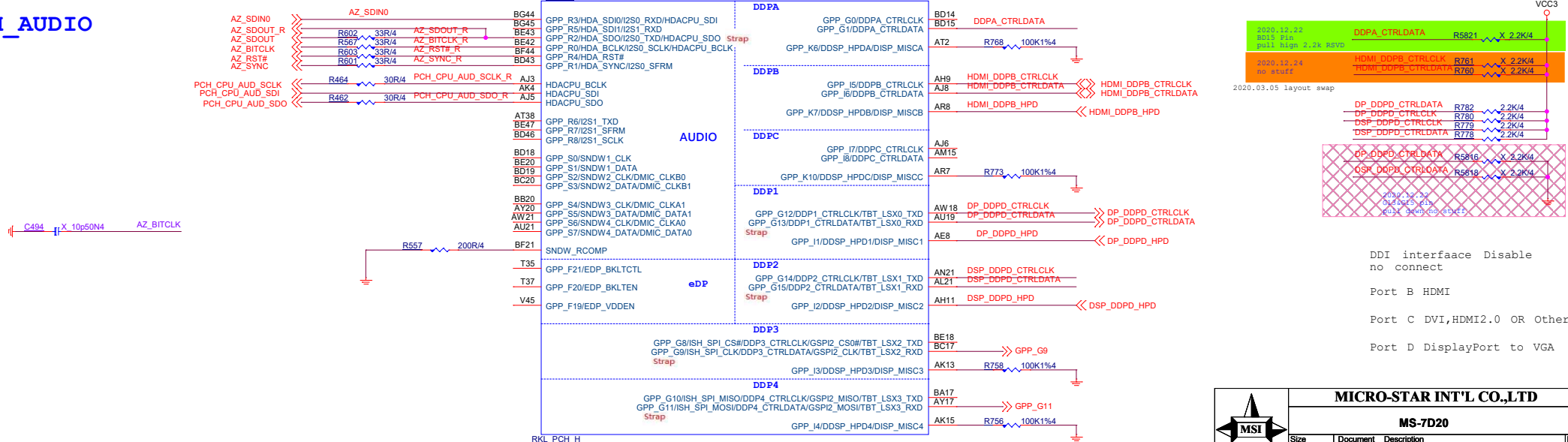




PCH CLK



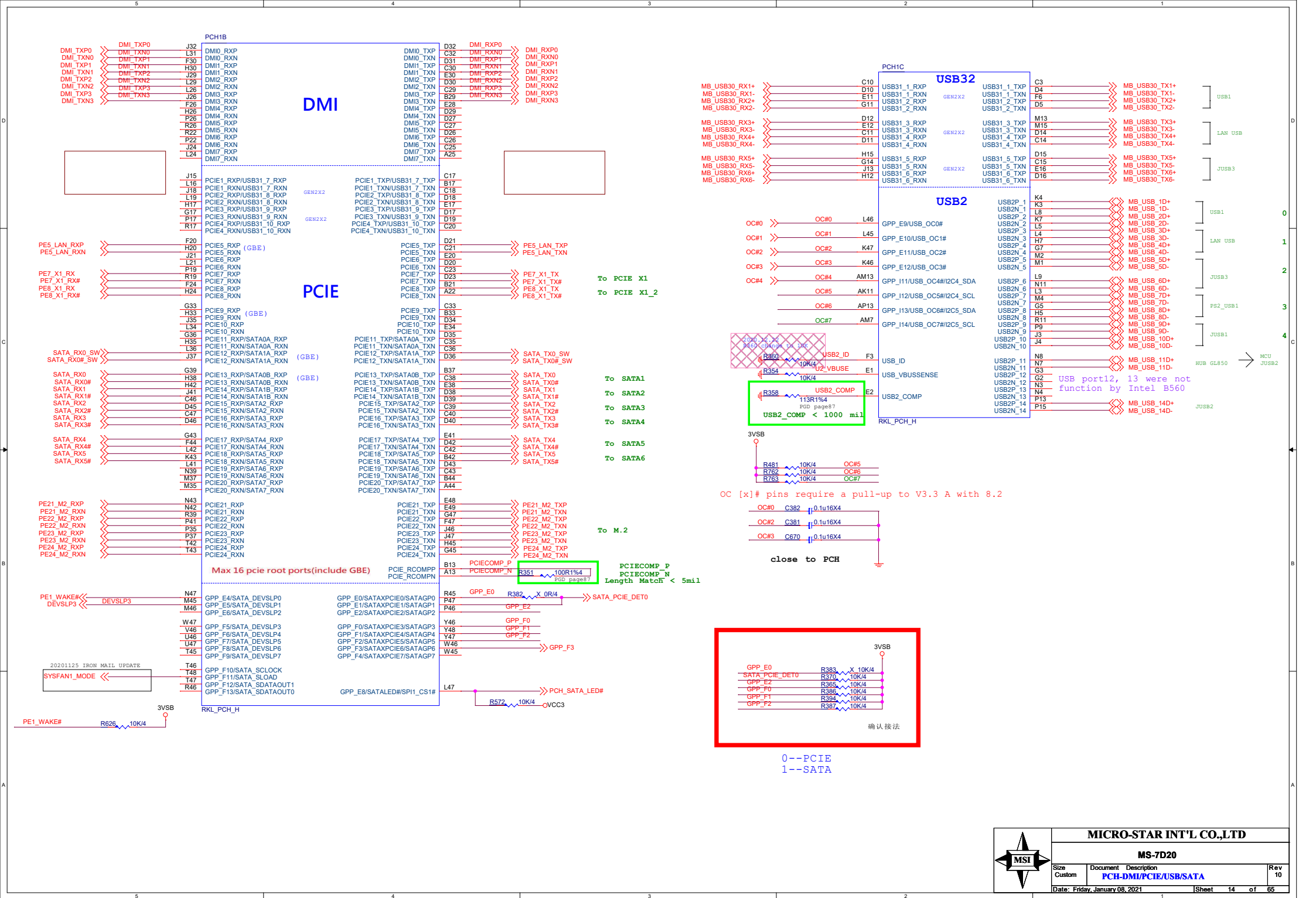
PCH AUDIO

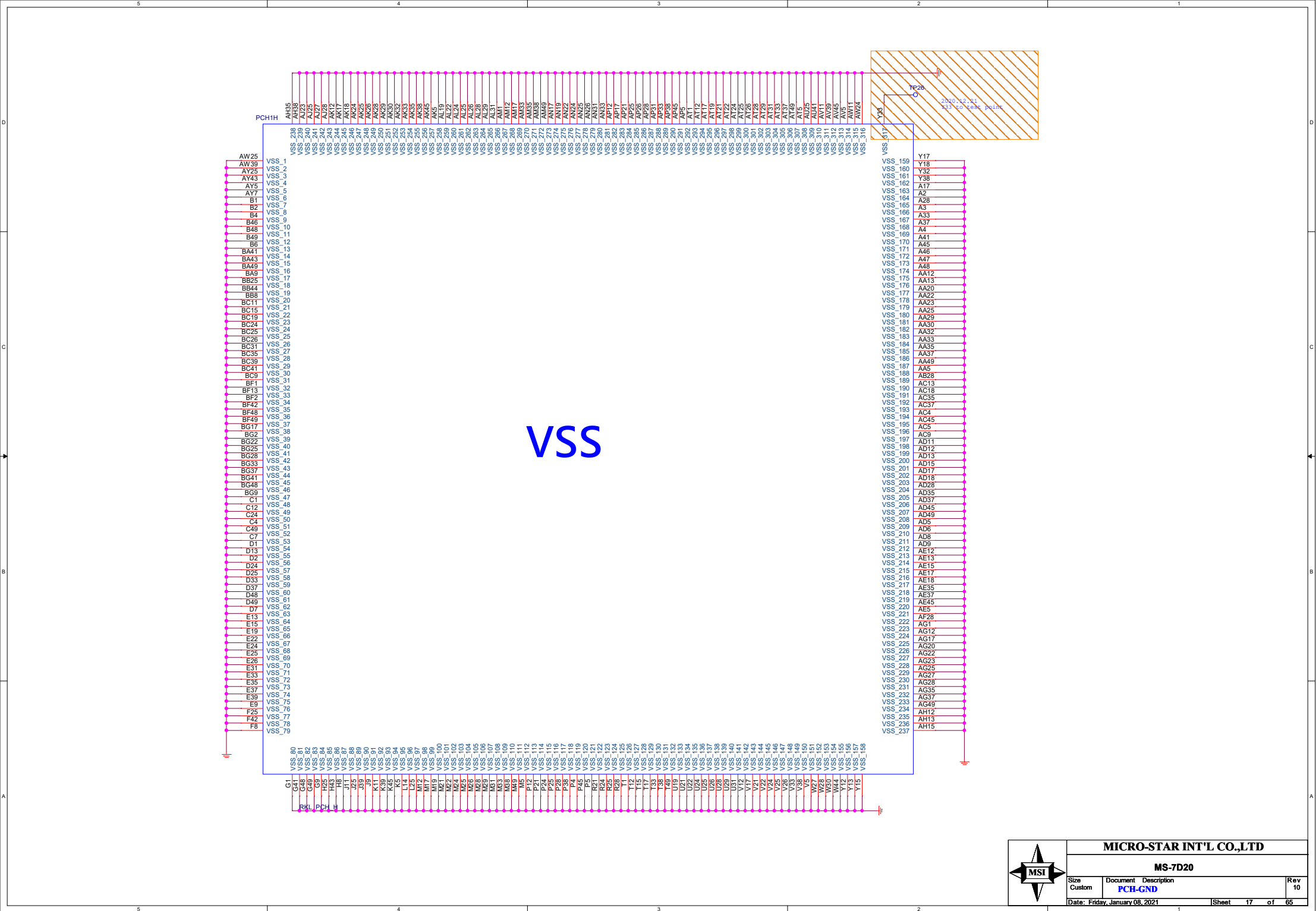


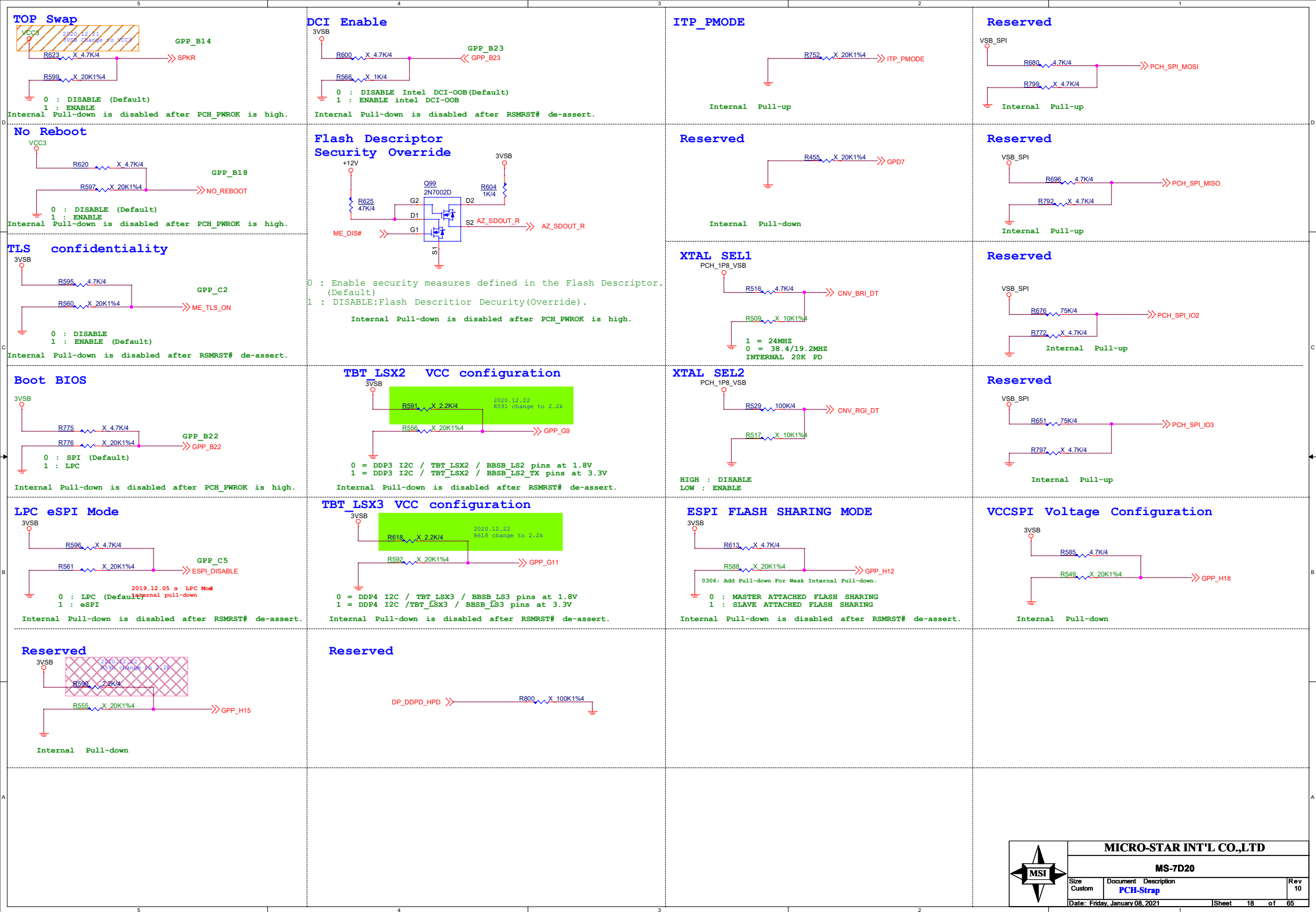
MICRO-STAR INT'L CO.,LTD

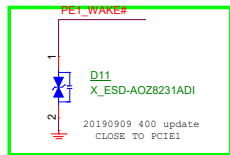
MS-7D20

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PCI Express X16 Slot

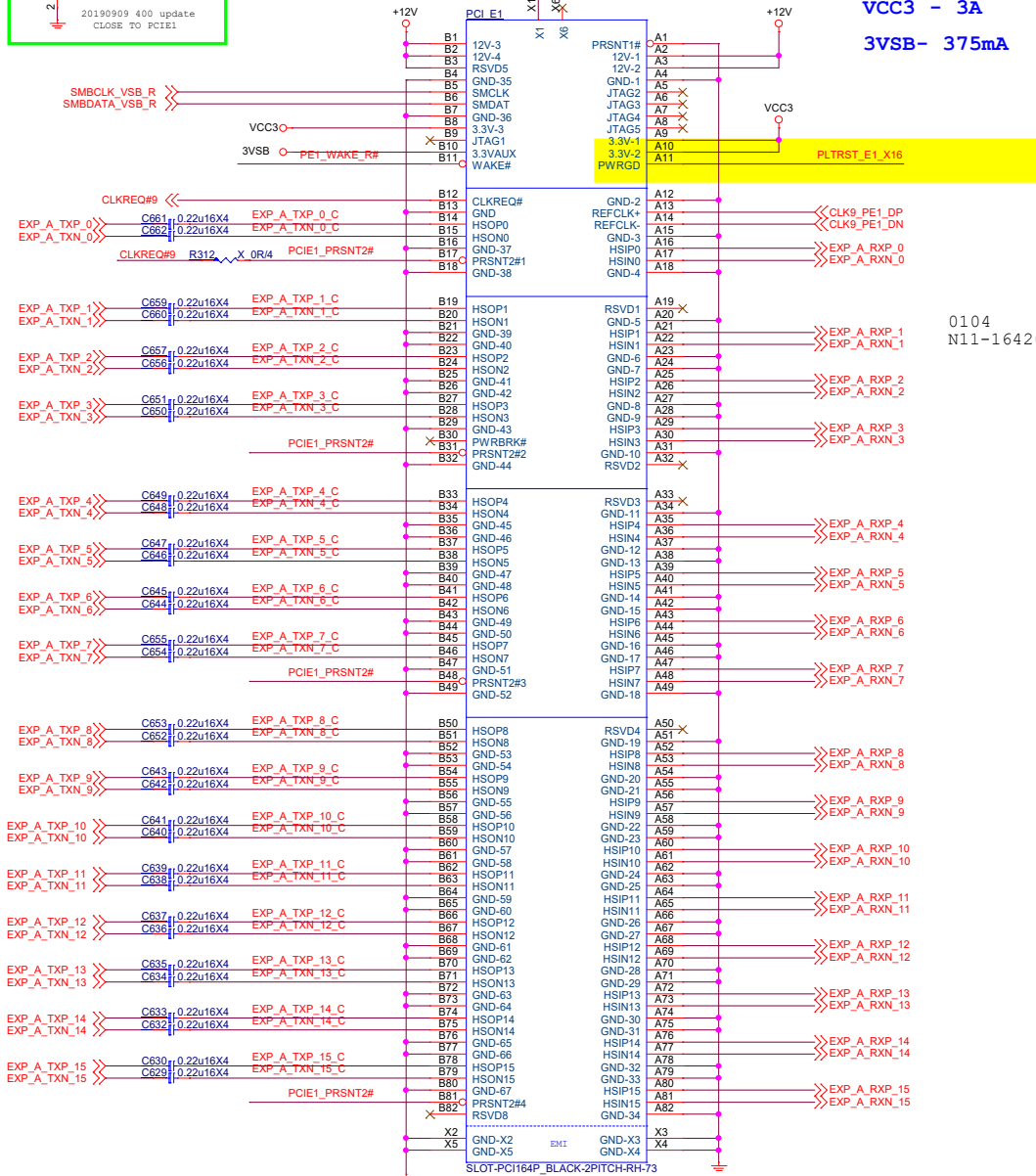
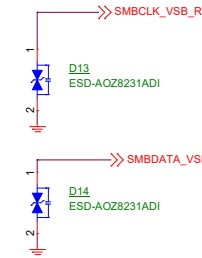
GEN3 OR GEN4?

12V - 5.5A

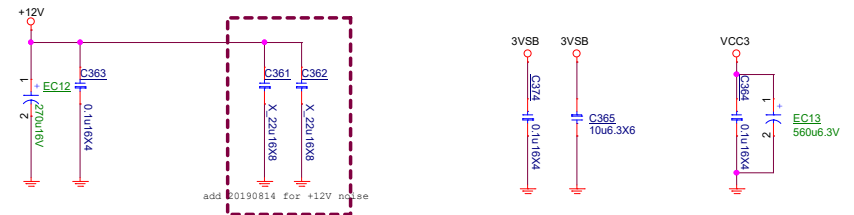
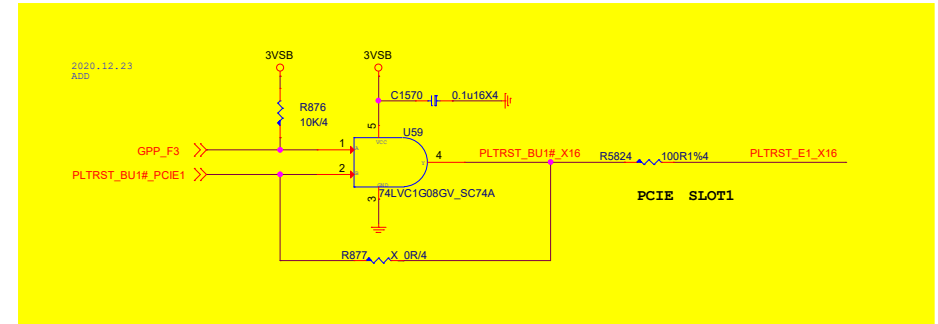
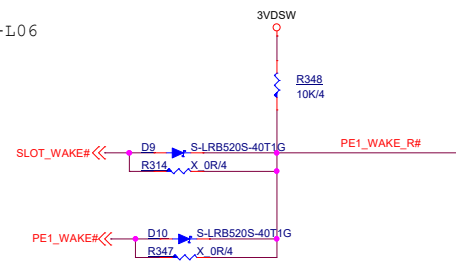
VCC3 - 3A

3VSB- 375mA

SMBus ESD

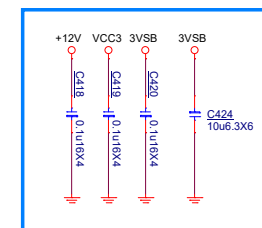
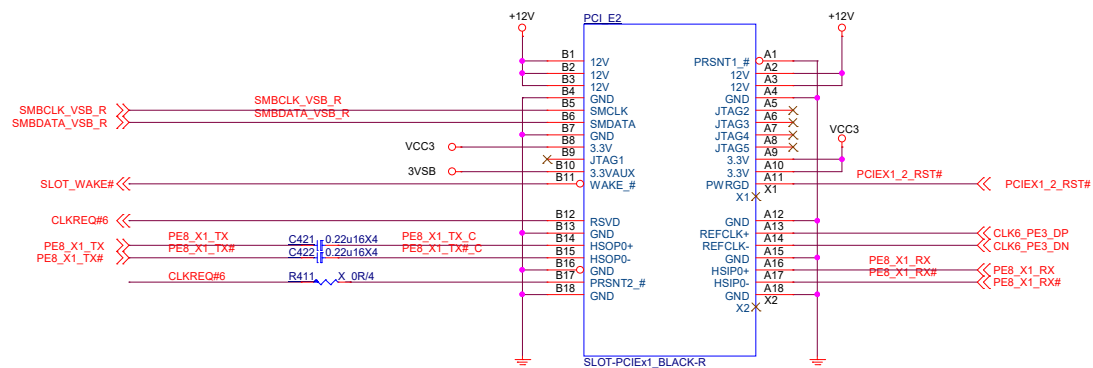
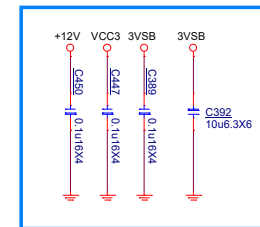
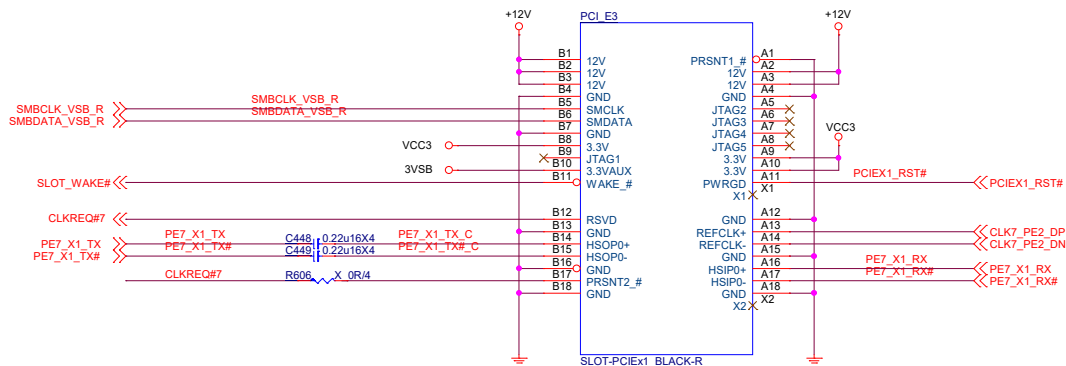


0104
N11-1642081-L06

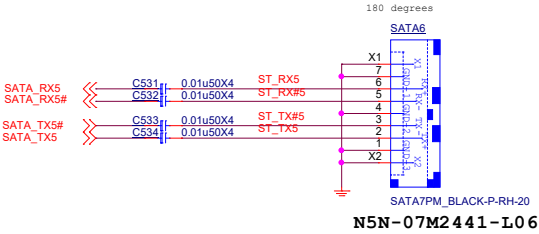
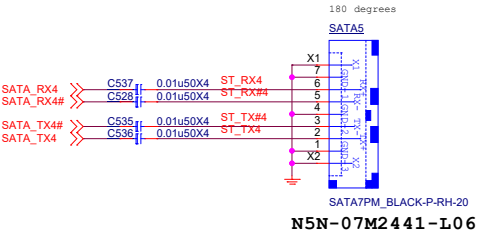
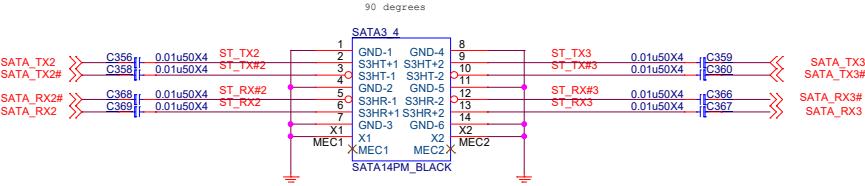
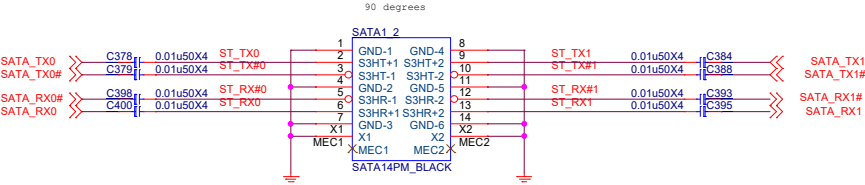


MICRO-STAR INT'L CO.,LTD				
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Custom		PCIE SLOT (X16)	10	
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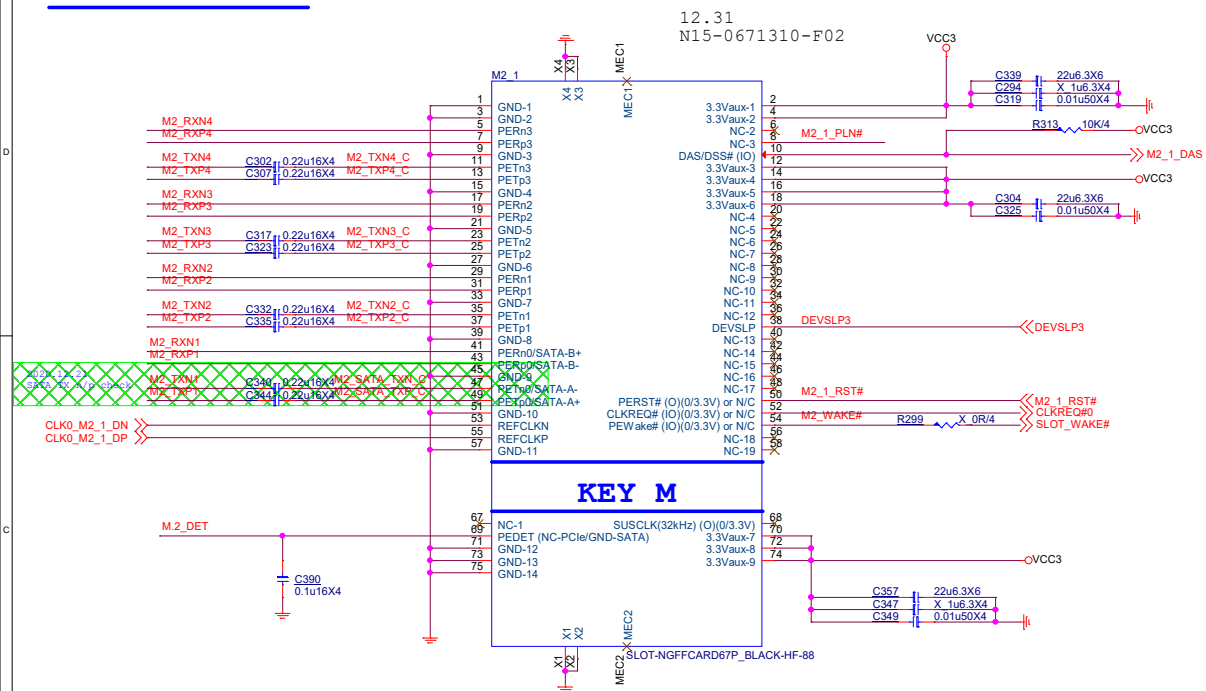
PCIE X1



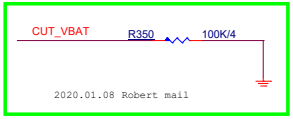
SATA Connector



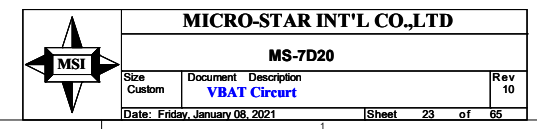
M.2 connector

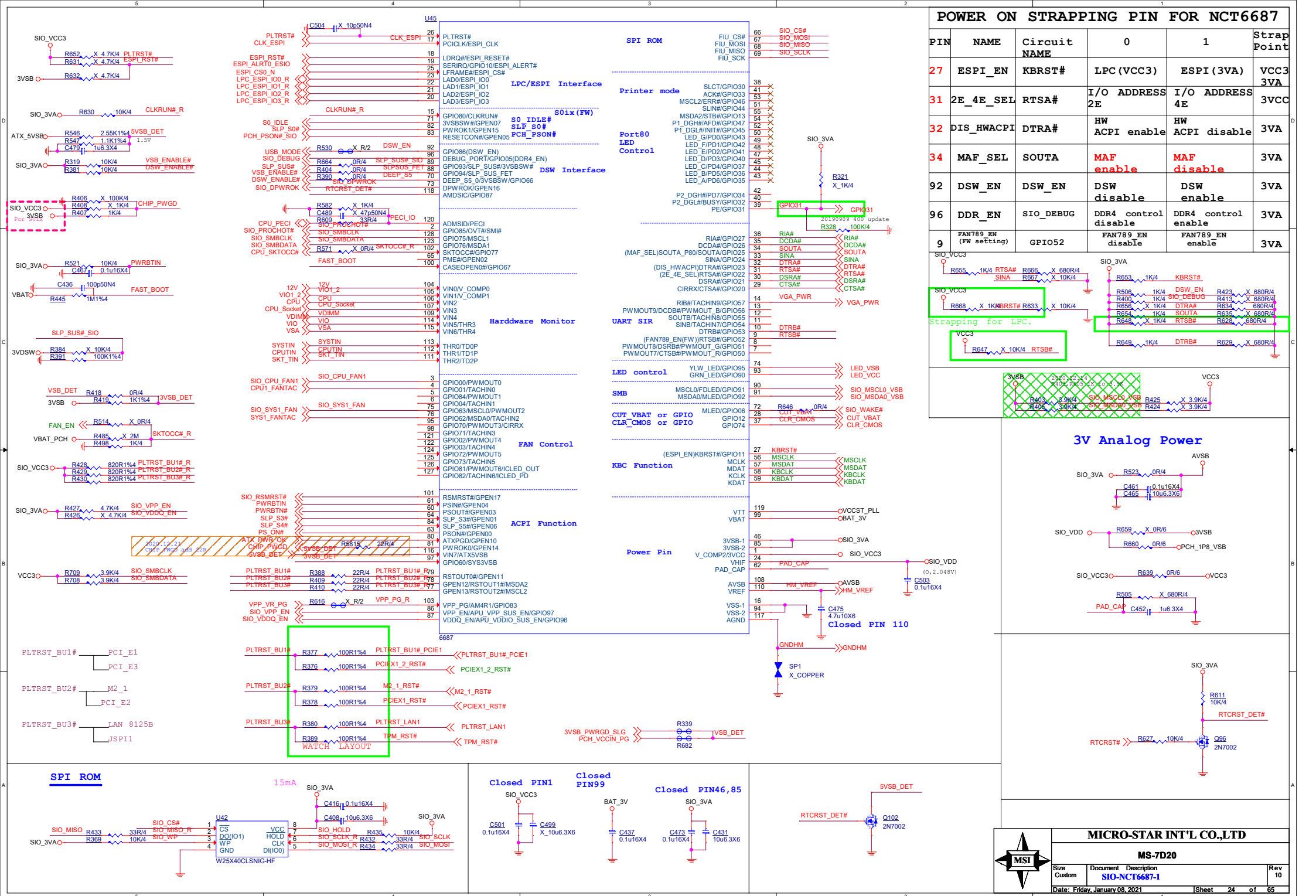


VBAT

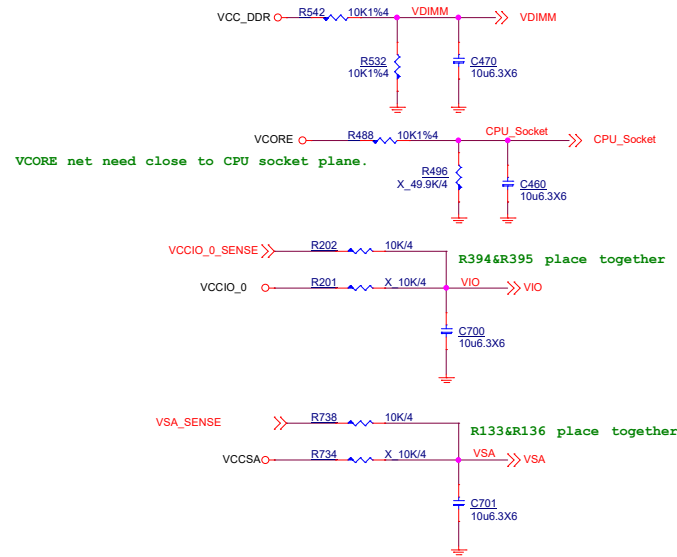
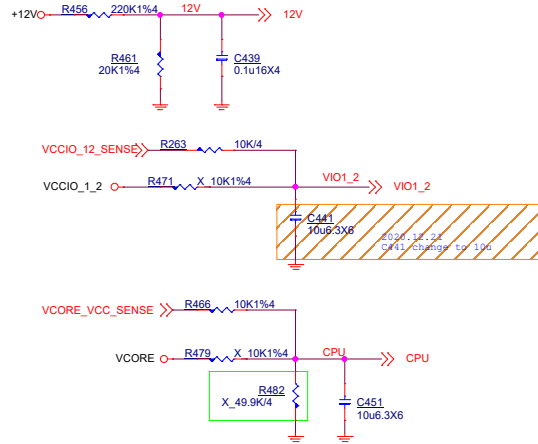
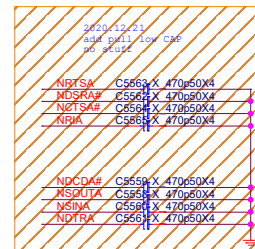
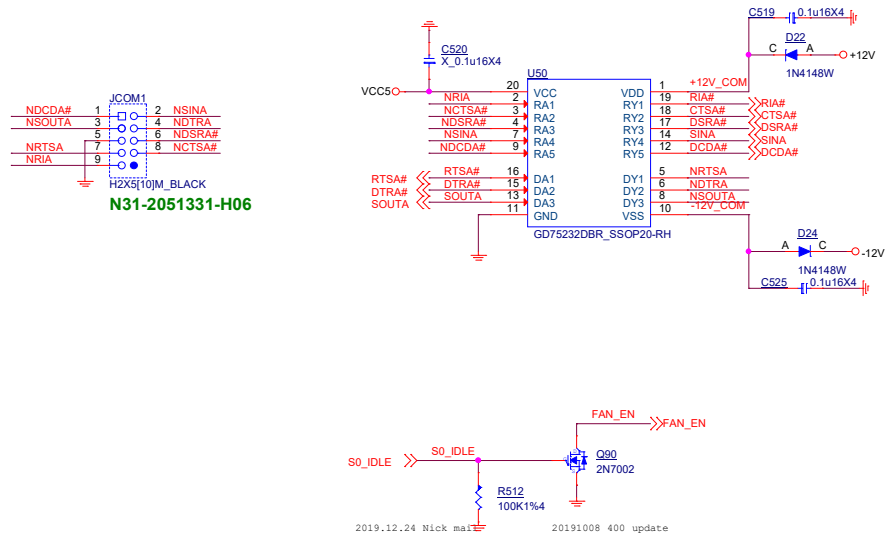


CLEAR CMOS

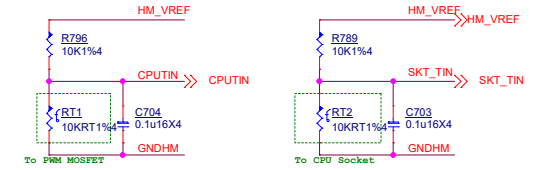
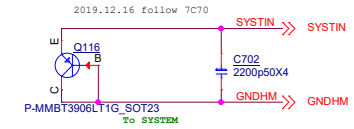




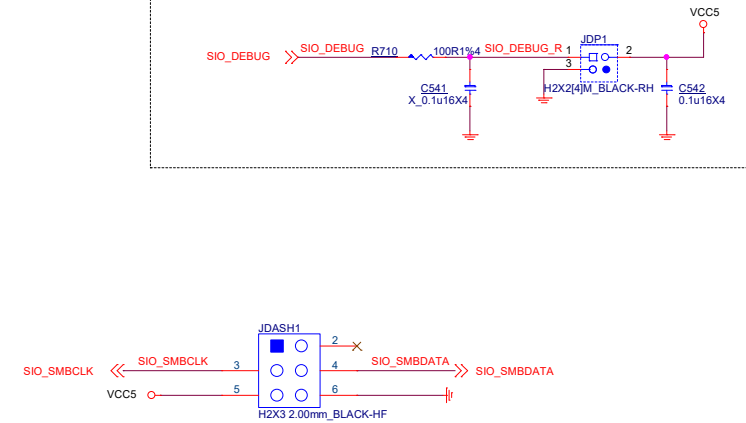
SIO HM Voltage Over 2V will Not Detect

**COM Port**

Thermal



DEBUG PORT



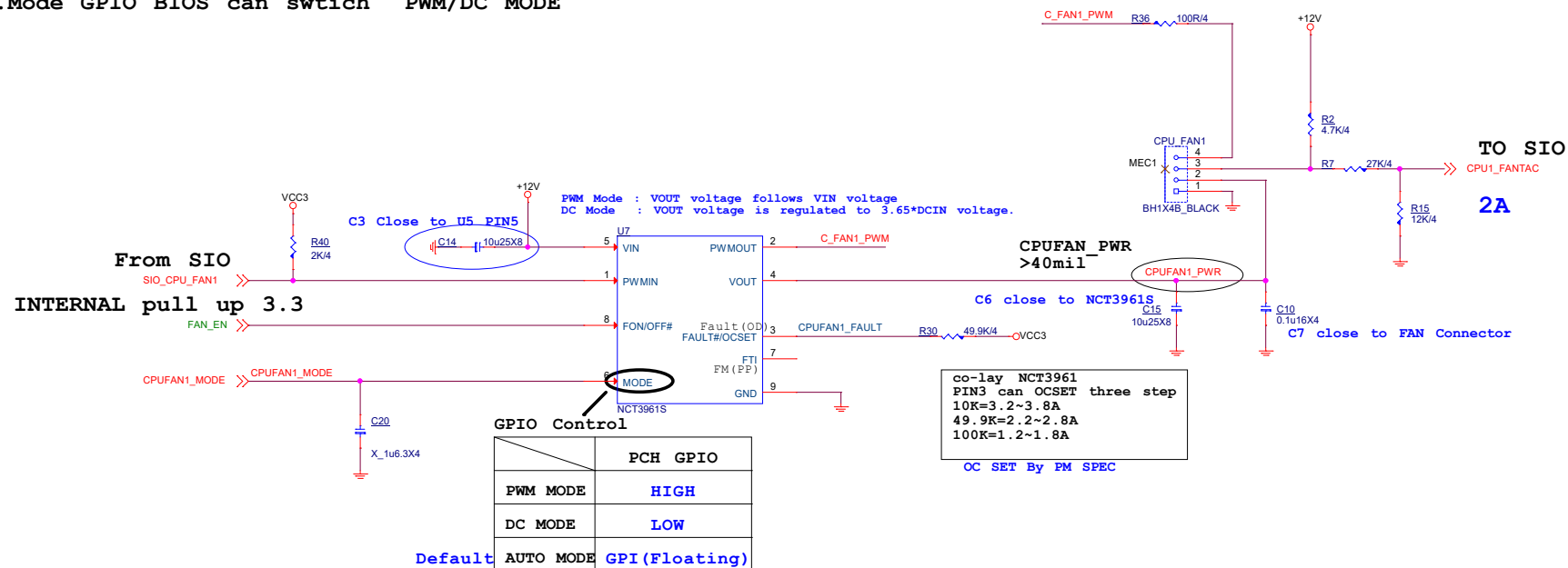
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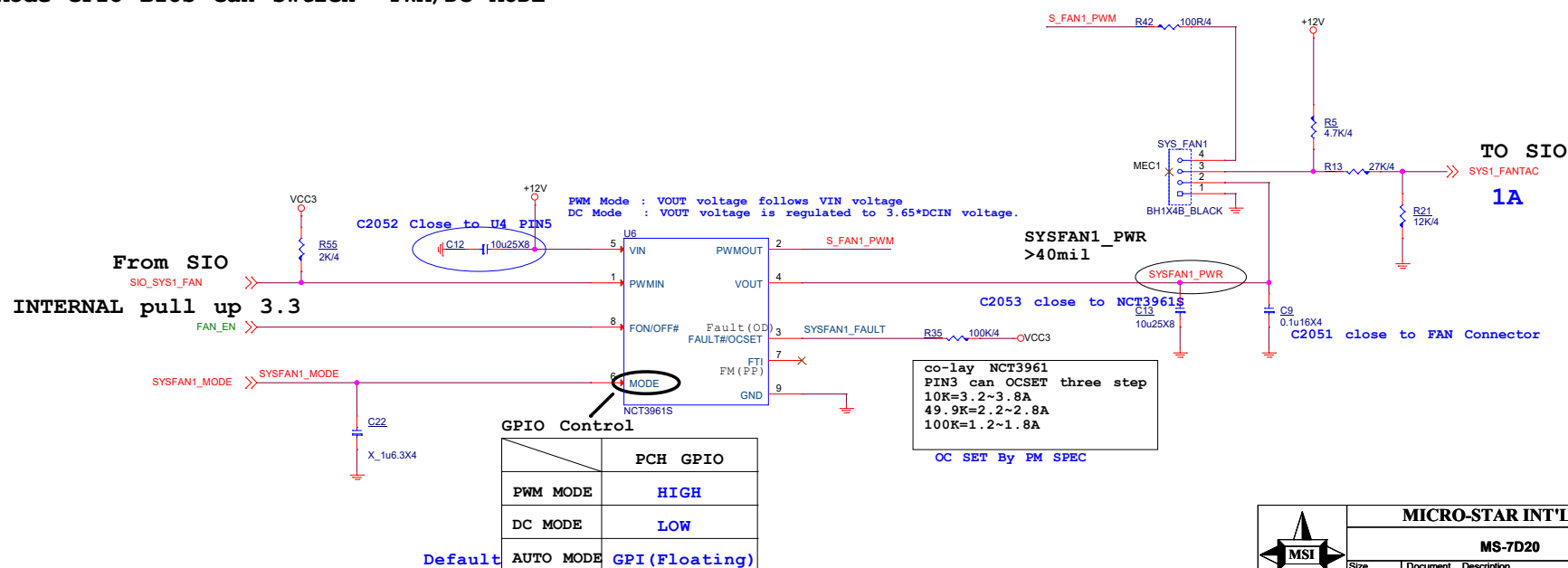
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



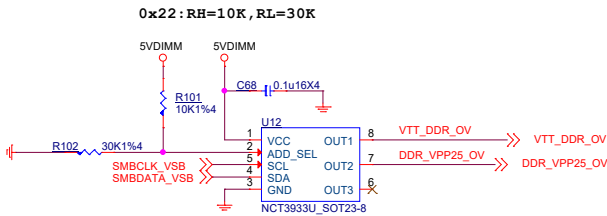
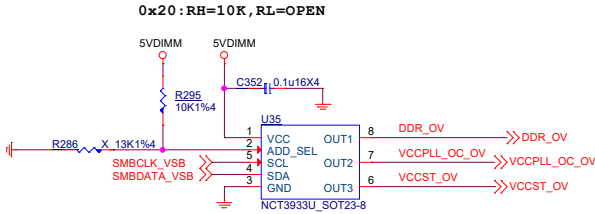
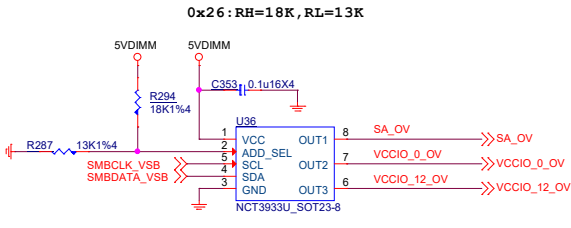
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

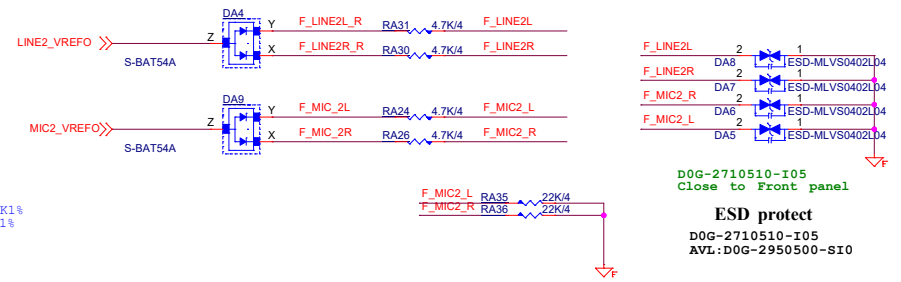
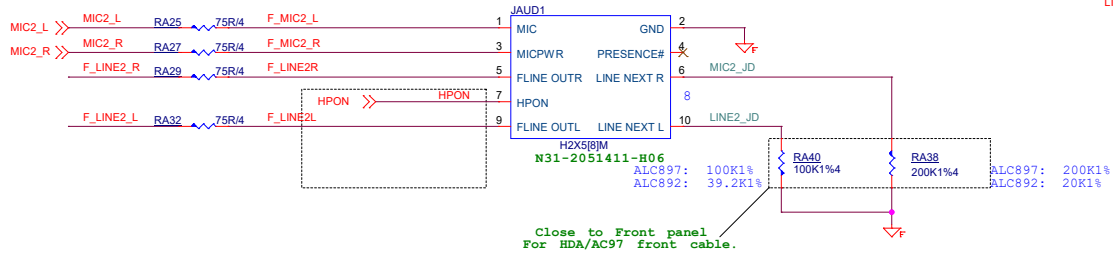
1.Mode GPIO BIOS can swtich PWM/DC MODE



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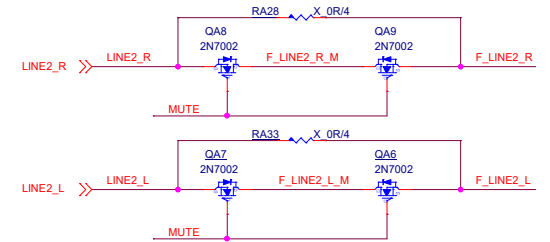
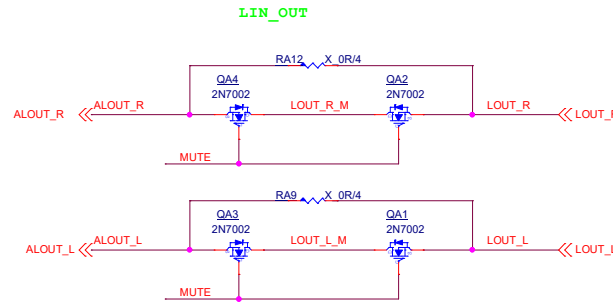
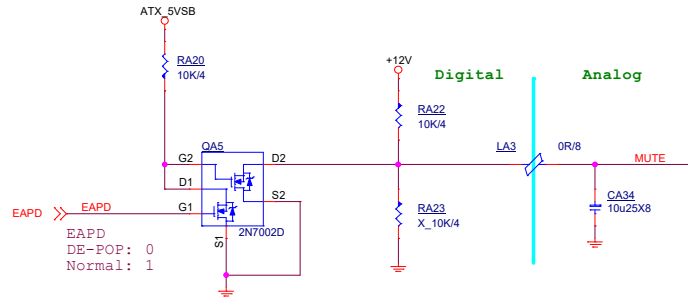
VOLTAGE CONSOLE





D0G-2710510-I05
Close to Front panel
ESD protect
D0G-2710510-I05
AVL:D0G-2950500-S10

De-POP circuit

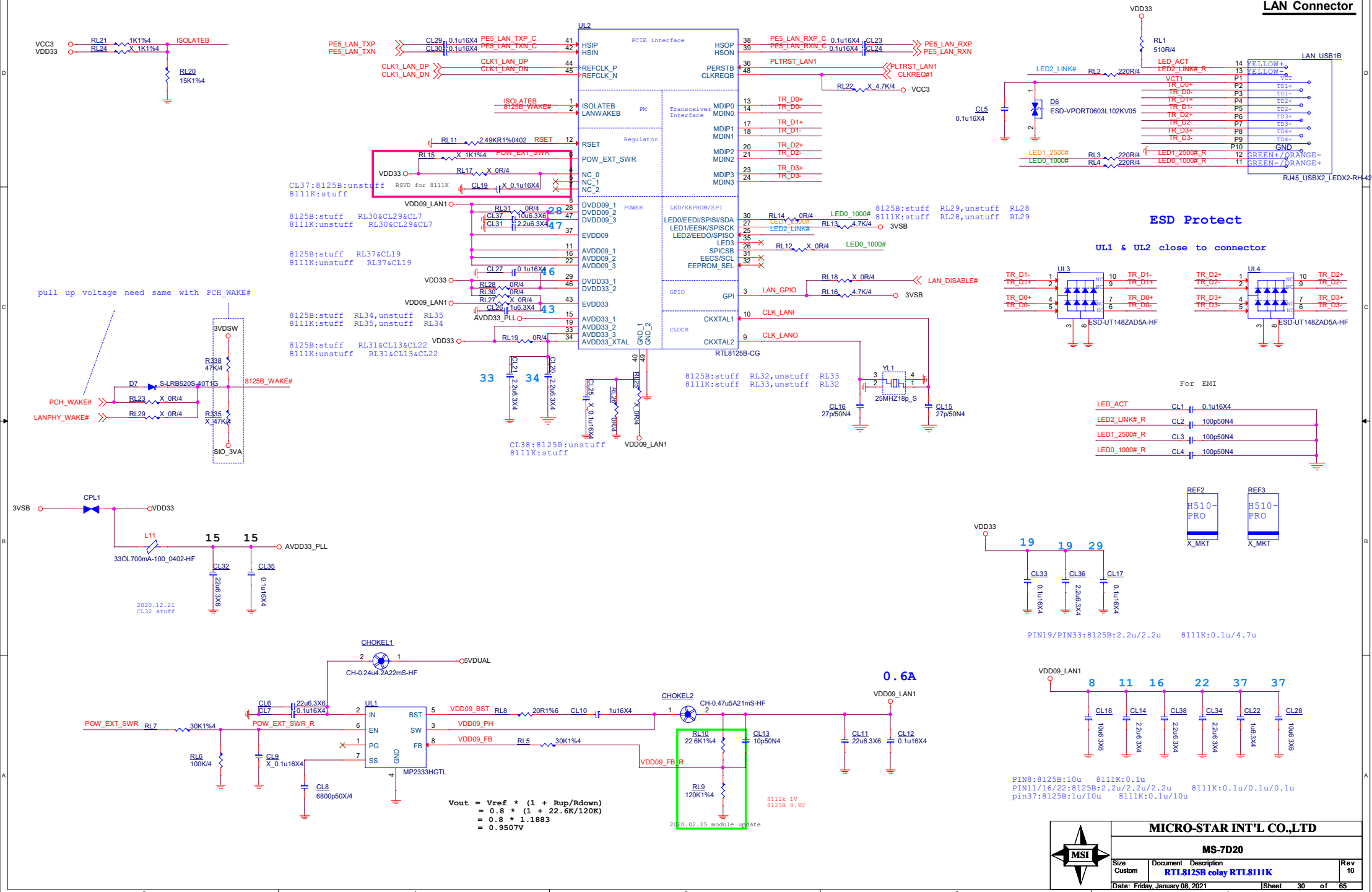


MICRO-STAR INT'L CO.,LTD

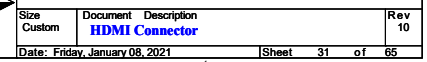
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Realtek Lan-RTL8125B/RTL8111K



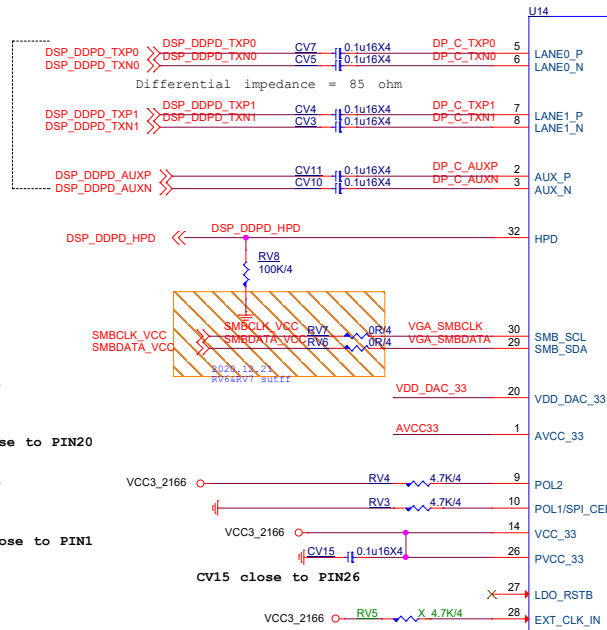
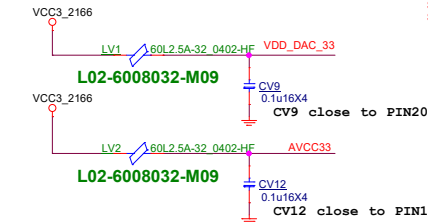
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



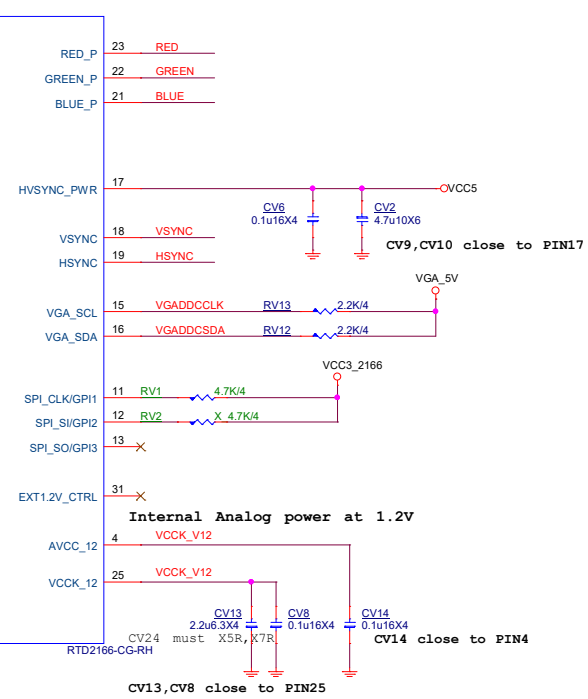
Note: If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

SMBus 0x68

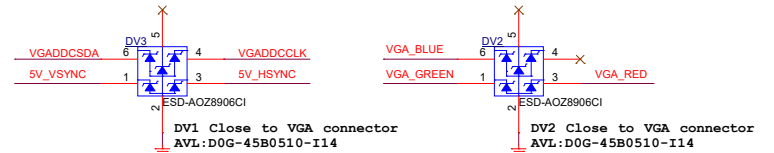
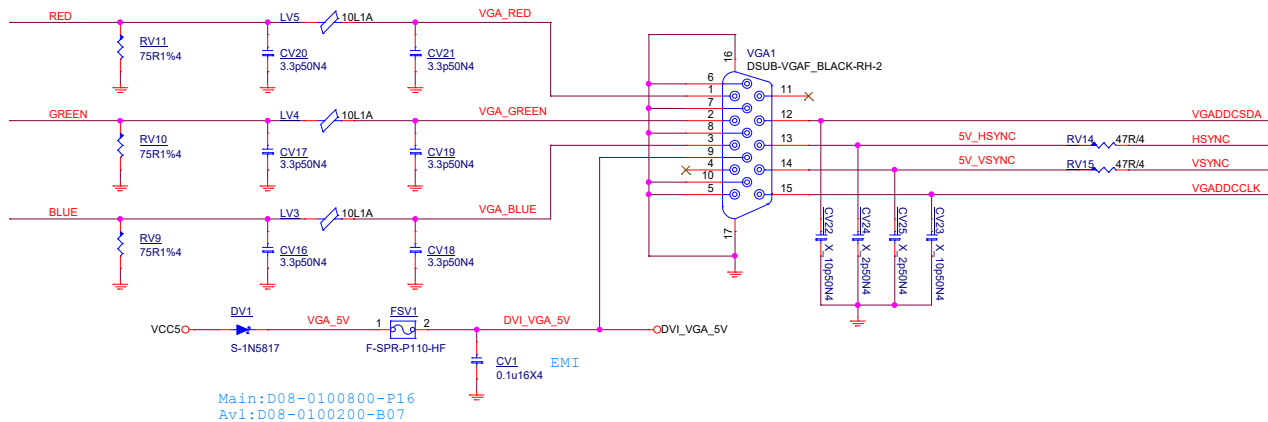
VCC3 Full Screen current 165mA



RTD2166



$$\begin{aligned} \text{Power Loss} &= (V_{in} - V_{out}) \cdot I_{out} \\ &= (5 - 3.389) \cdot 0.17 \\ &= 1.611 \cdot 0.17 \\ &= 0.274W < 0.4W \end{aligned}$$



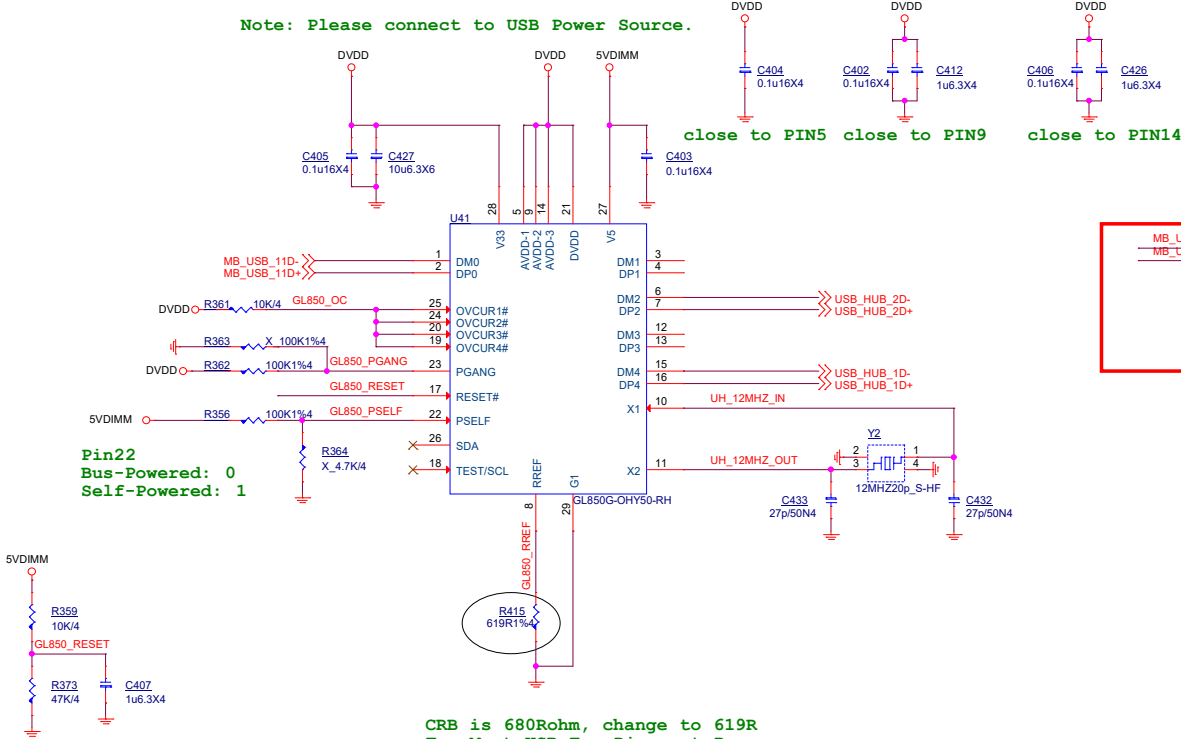
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Rear USB2.0 HUB

Pin23
Gang input:1
Individual input:0

Pin22
Bus-Powered: 0
Self-Powered: 1

Note: Please connect to USB Power Source.

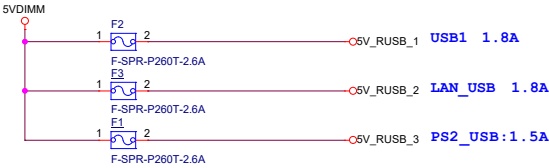


MB_USB_11D- R746 X 0R/4 MB_USB_HUB_R- R749 X 0R/4 USB_HUB_1D-
MB_USB_11D+ R747 X 0R/4 MB_USB_HUB_R+ R748 X 0R/4 USB_HUB_1D+
R5797 R5798 R5806 R5807 STUFF
ONLY B560M-A PRO (WITHOUT MCU)
PUT ON THE BOTTOM

CRB is 680Rohm, change to 619R
For Meet USB Eye Diagramt Pass.

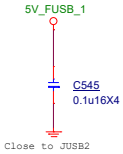
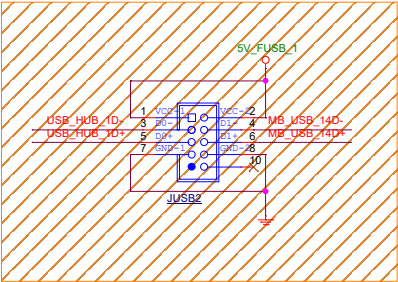
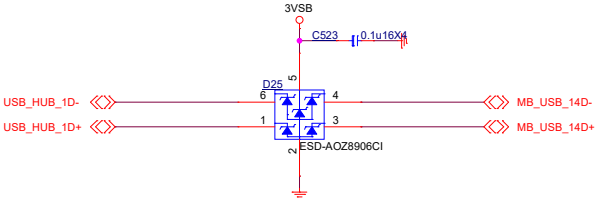
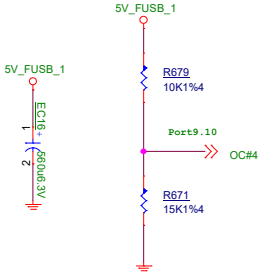
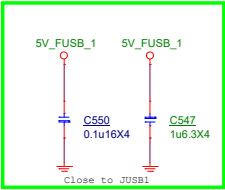
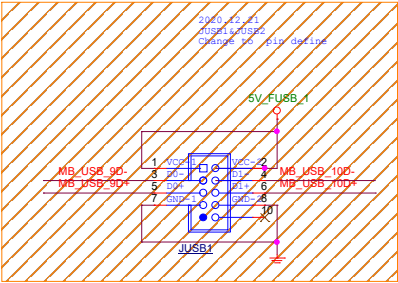
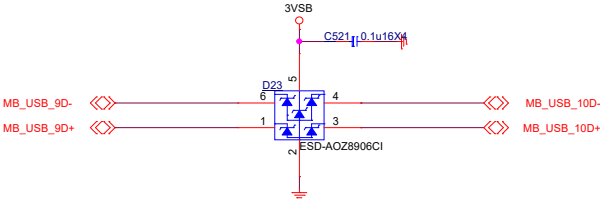
Note: USB2.0 Hub no need mapping OC# to PCH, Hub can report to PCH by Self.

REAR USB PORT POWER



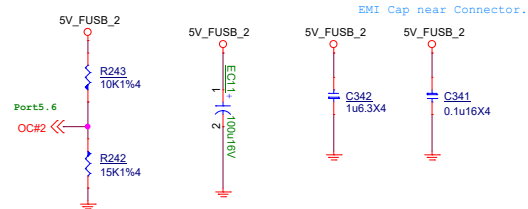
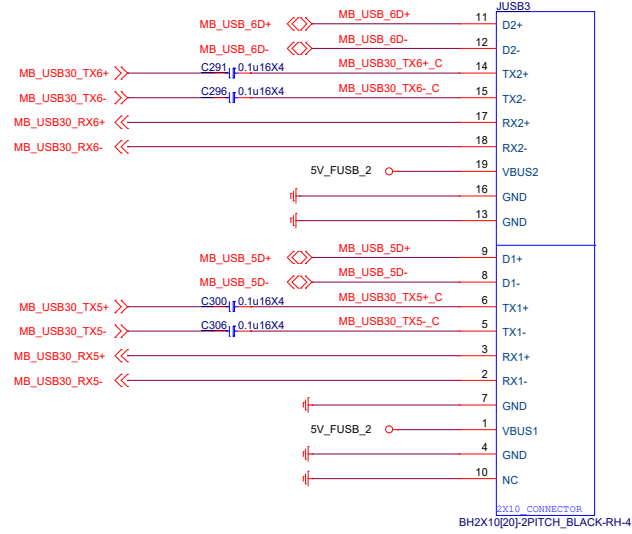
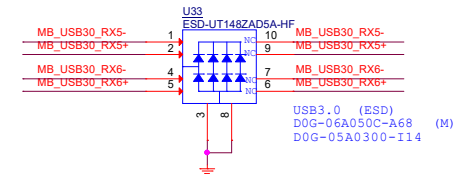
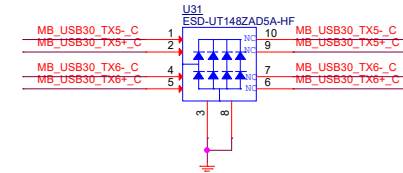
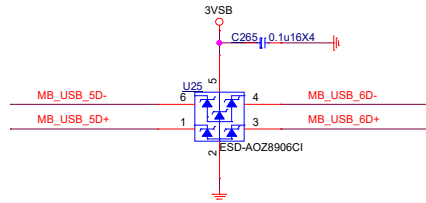
FRONT USB PORT POWER





Front USB3

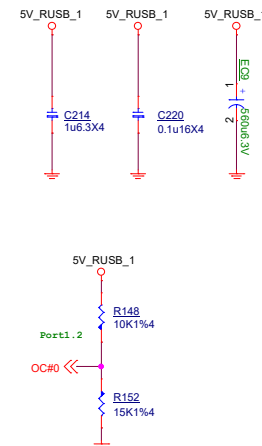
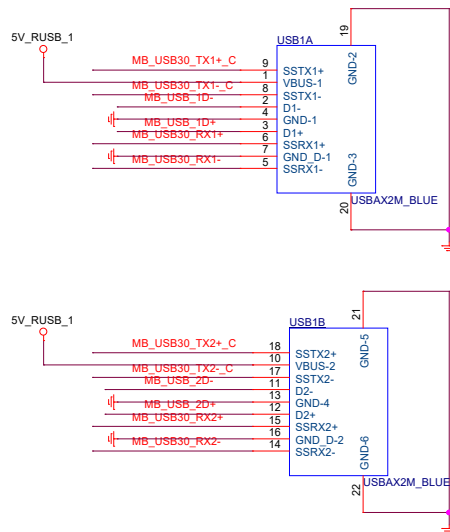
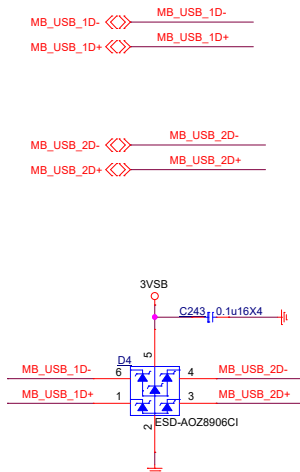
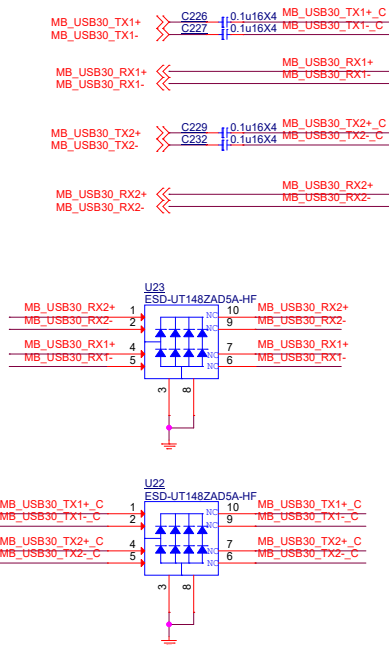
1.8A



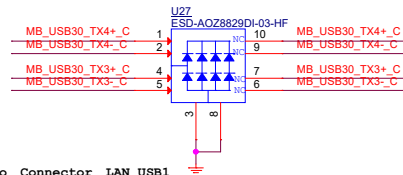
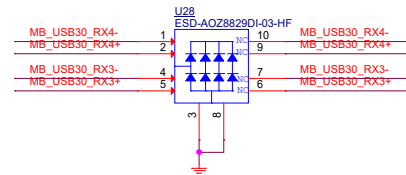
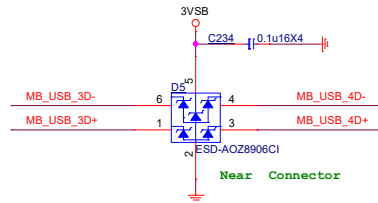
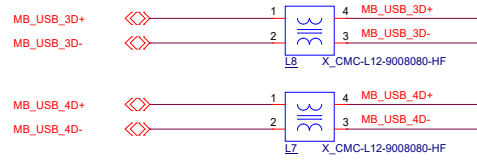
Rear USB3.0

USB3.0 Port1.2
USB2.0 Port1.2

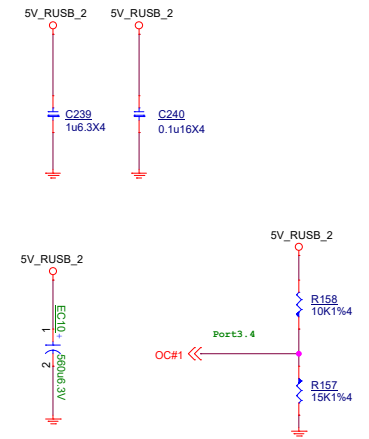
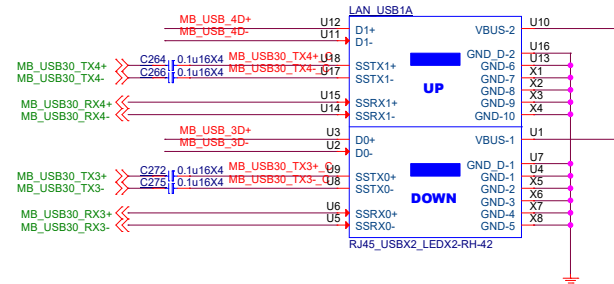
1.8A




```
20200721 keep common choke footprint and default short
```



close to Connector LAN_USB1

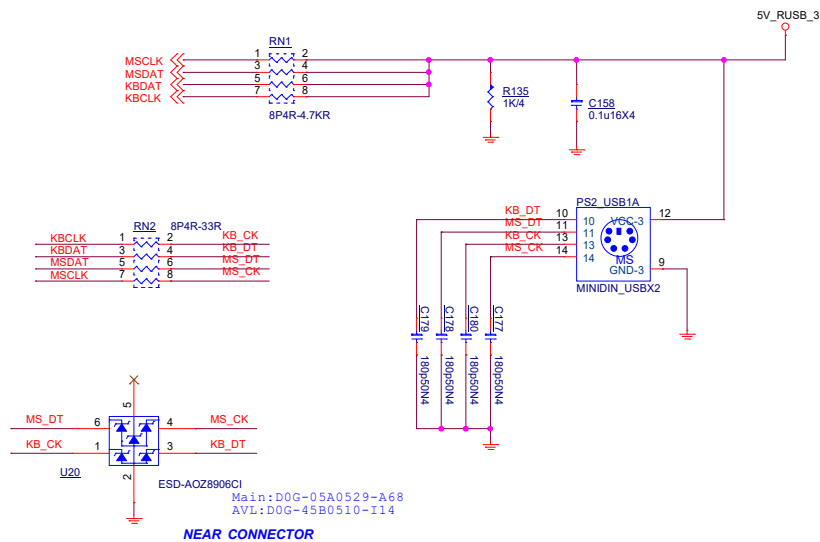
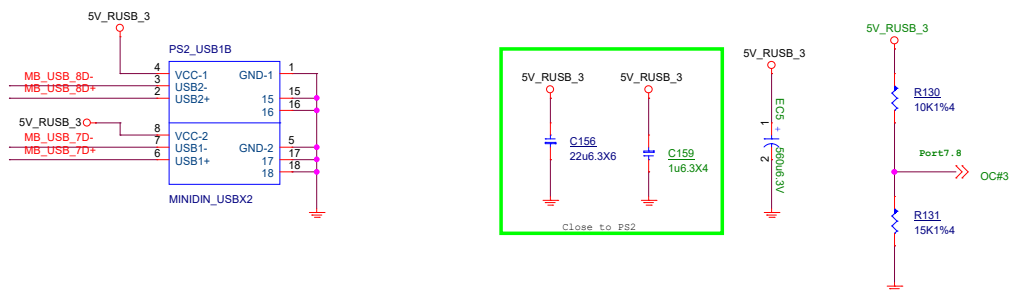


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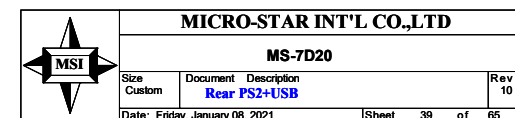
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PS2 Connector 0.5A

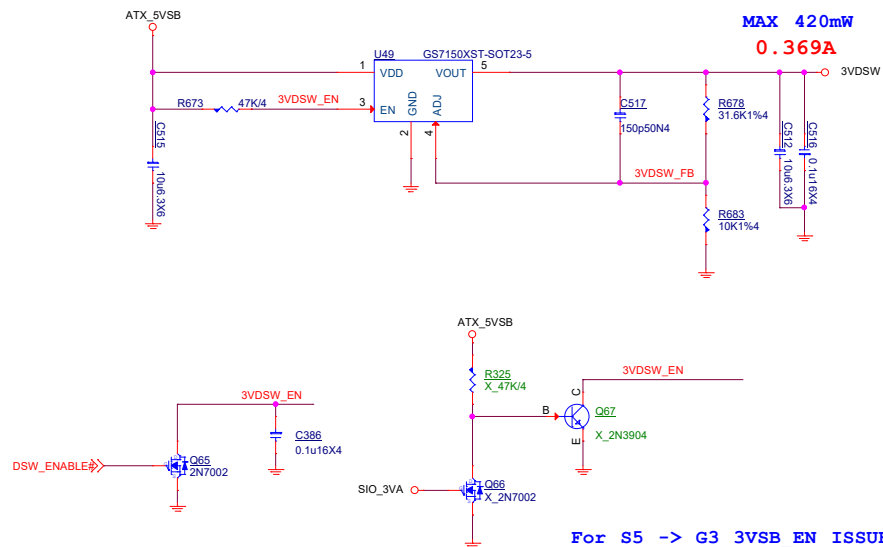
**PS2 USB Connector** 1.0A

20200721 keep common choke footprint and default short



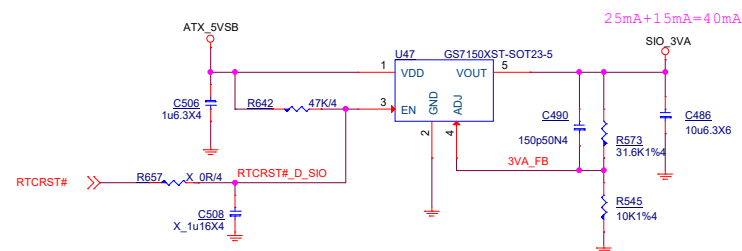
3VDSW

$$\begin{aligned} \text{Power Loss} &= (V_{in} - V_{out}) * I_{out} \\ &= (5 - 3.3) * 0.369 \\ &= 1.7 * 0.369 \\ &= 0.6273W > 0.42W \end{aligned}$$



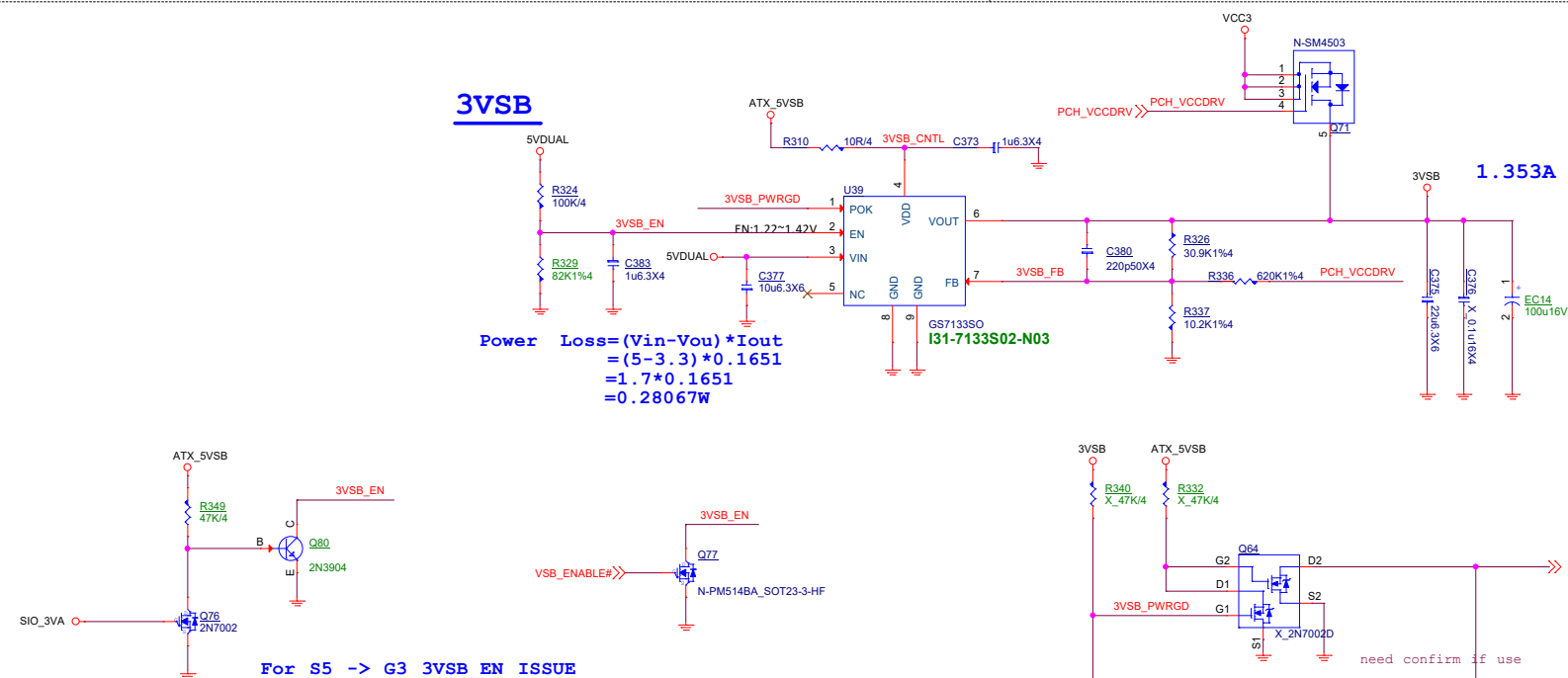
SIO 3VA

$$\begin{aligned} \text{Power Loss} &= (V_{in} - V_{out}) * I_{out} \\ &= (5 - 3.3) * 0.04 \\ &= 1.7 * 0.04 \\ &= 0.068W \end{aligned}$$



3VSB

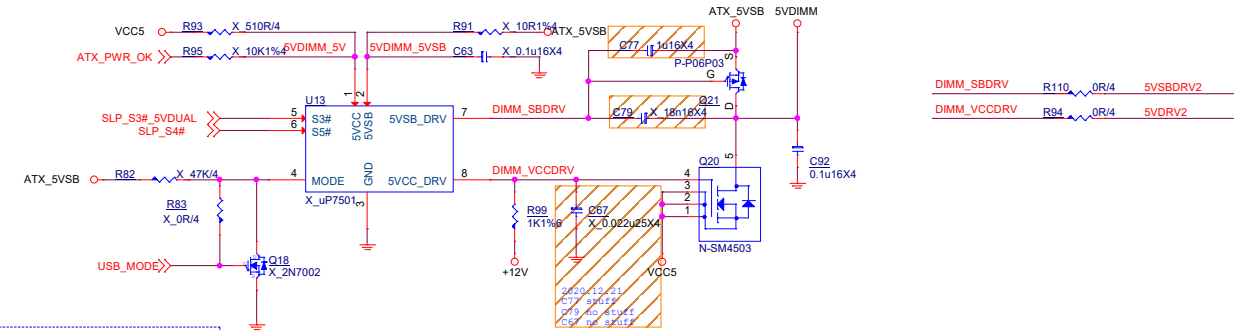
$$\begin{aligned} \text{Power Loss} &= (V_{in} - V_{out}) * I_{out} \\ &= (5 - 3.3) * 0.1651 \\ &= 1.7 * 0.1651 \\ &= 0.28067W \end{aligned}$$



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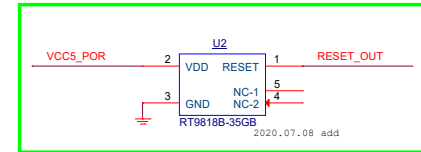
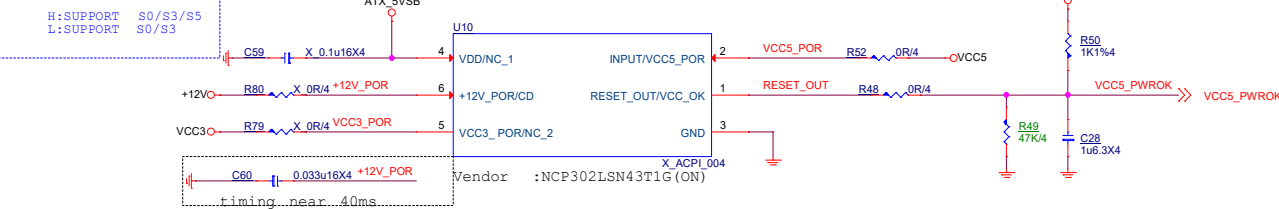
5VDDIMM FOR DDR

14.36A



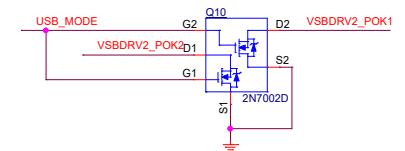
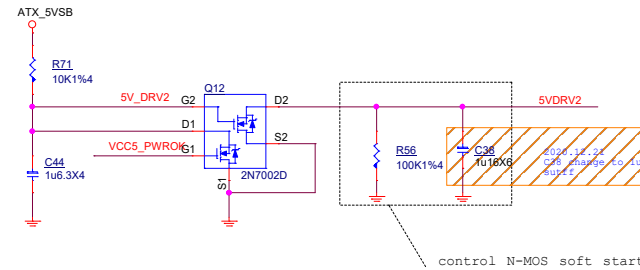
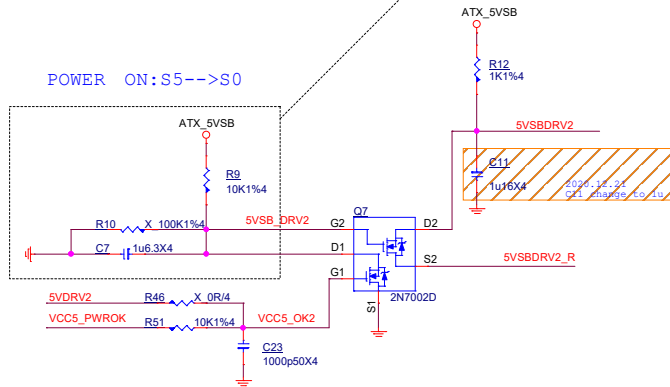
TO:NCT6687 GP86

5VDDIMM COLAY

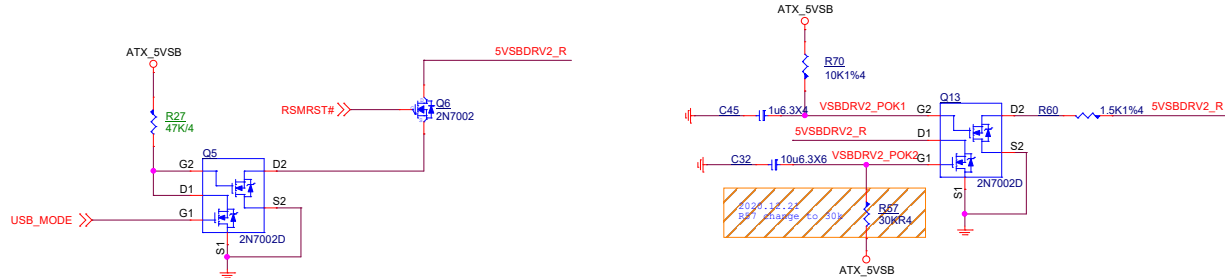
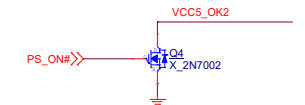


control P-MOS soft start and waiting ATX_5VSB ramp to 100%

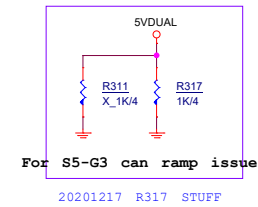
POWER ON:S5-->S0



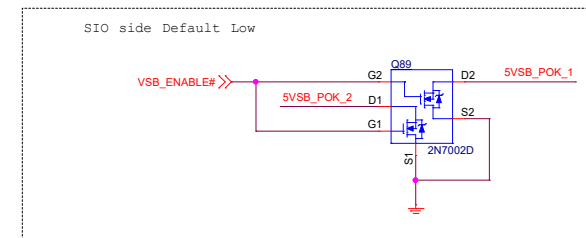
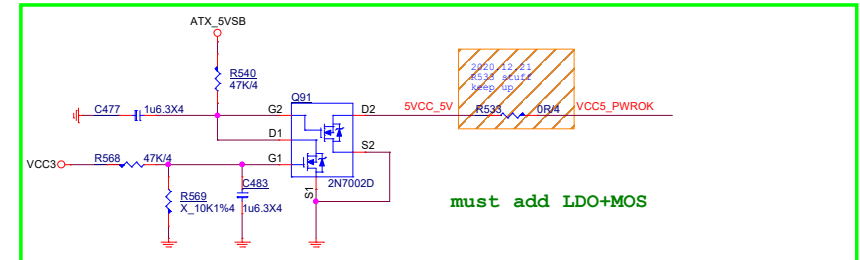
POWER OFF:S0-->S5



5VDUAL

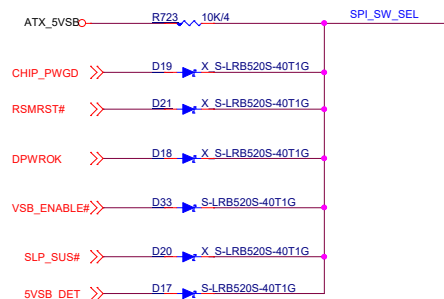


POWER ON:S5-->S0

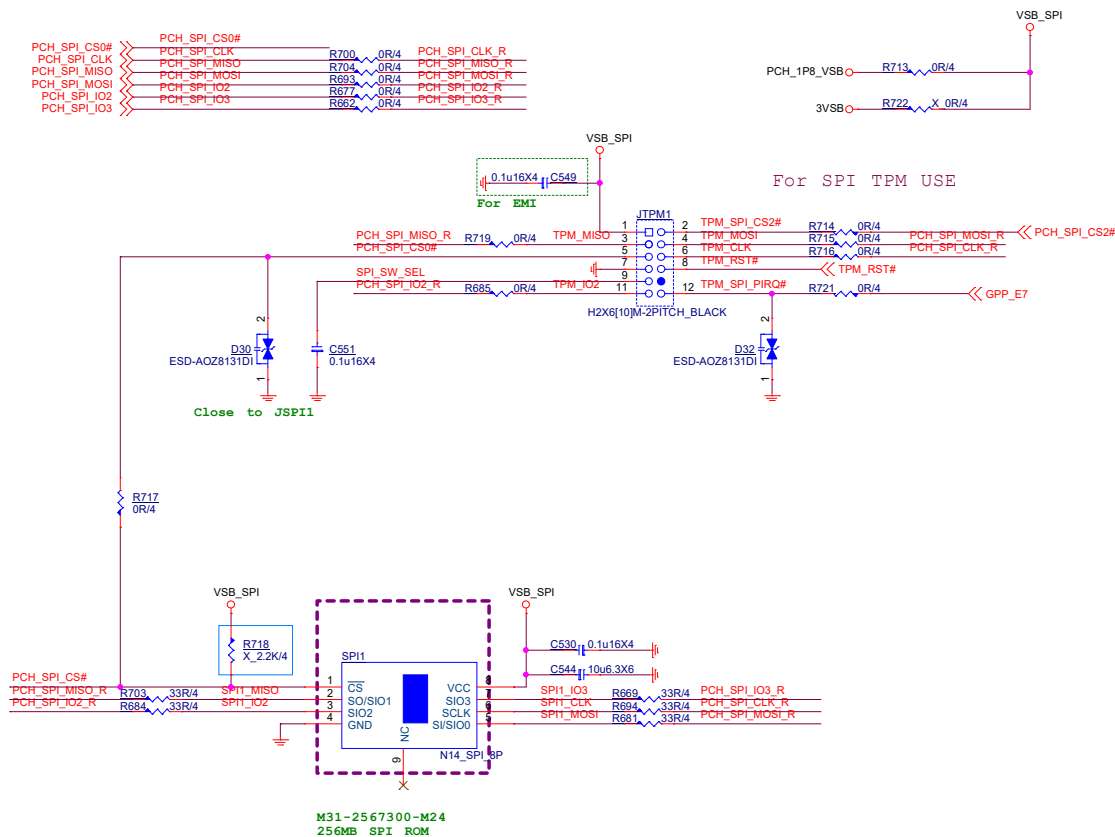
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Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.



For TL624-1.
DEEP Mode : Stuff D48/R2517
DSW Mode : Stuff D48/D49/R2517



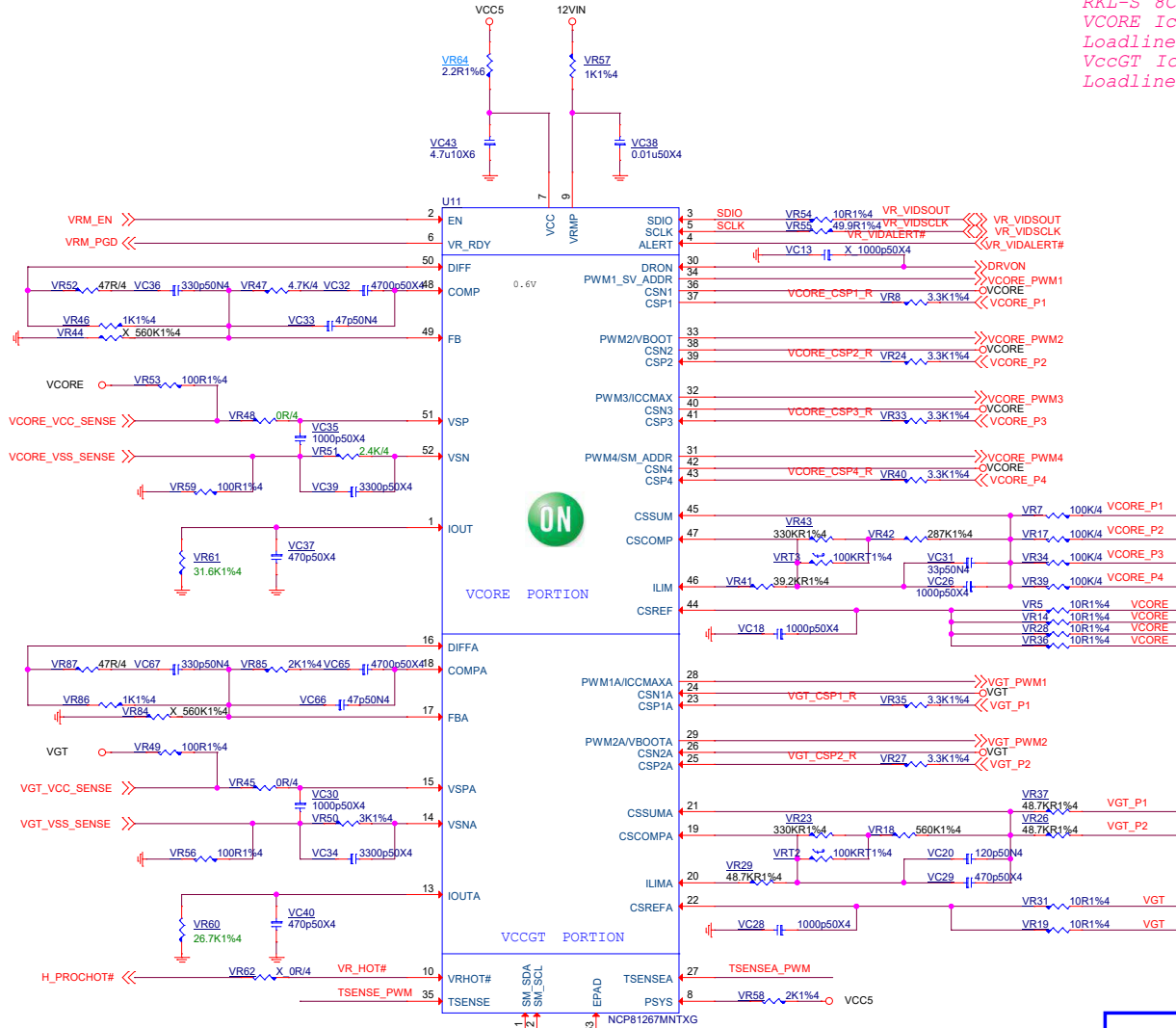
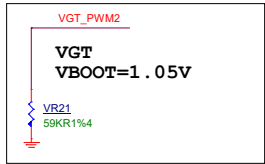
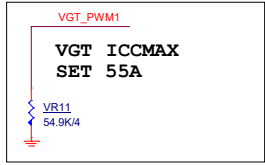
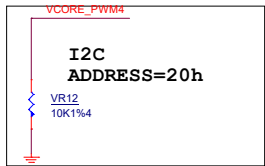
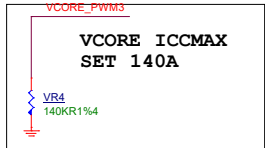
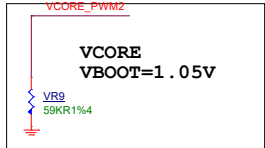
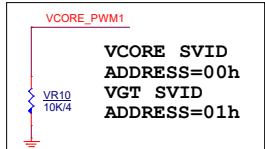
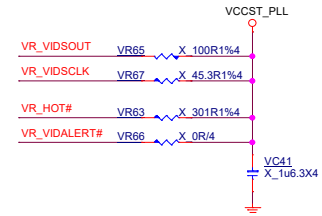
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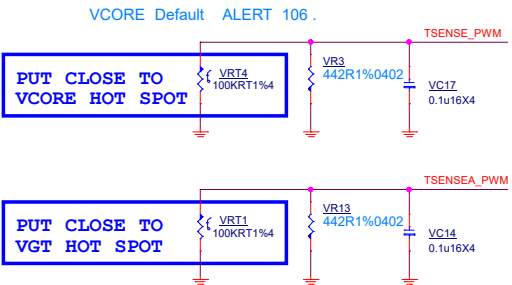
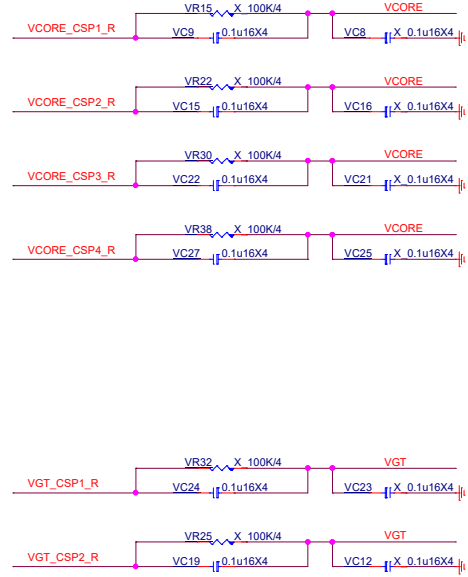
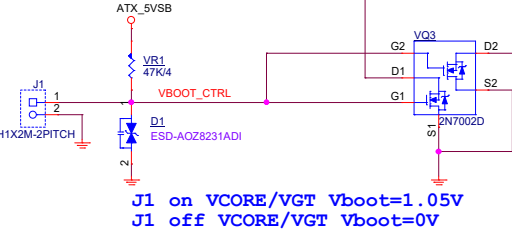
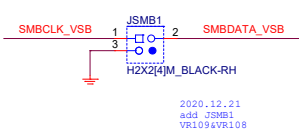
VCORE Iccmax 140A,TDC 132A, OCP182A.
VGT Iccmax 55A,TDC 46A, OCP76A.

SPEC:output choke CH-0.33u45A0.71mS-HF
RKL-S 8CORE 35W performance spec:
VCORE Iccmax =140A,
Loadline=1.1mohm
VccGT Iccmax=54A,PL2=46A
Loadline=4 mohm

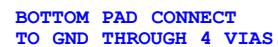
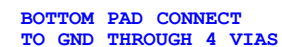


Fsw default=180Khz,CAN BE
program up to 1.17Mhz VIA I2C.

BOTTOM PAD CONNECT
TO GND THROUGH 6 VIAS



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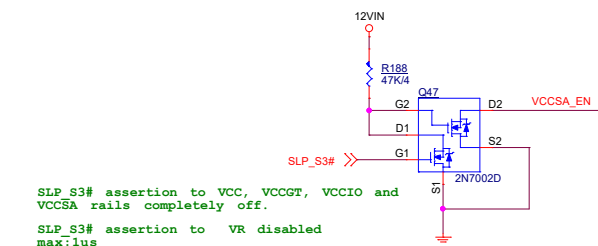
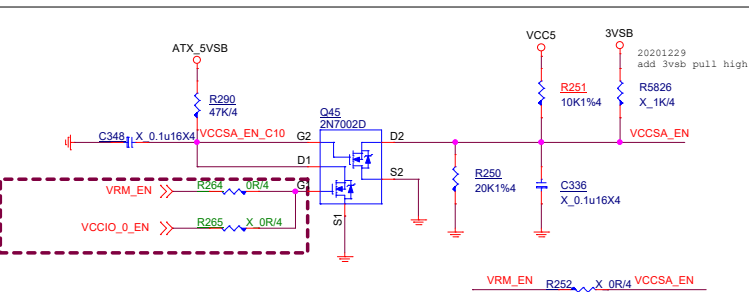
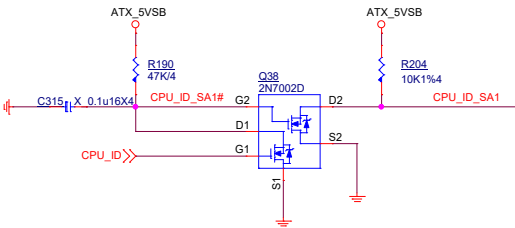
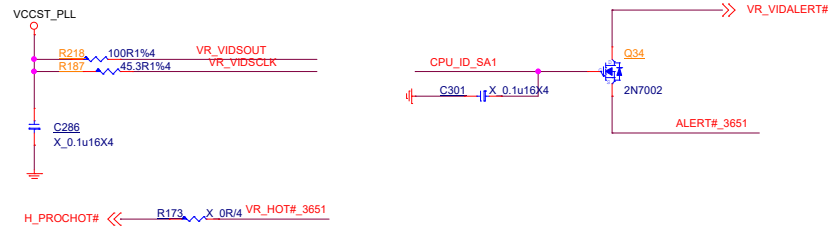


On suggest, C5616 need be place close to output choke to reduce ripple.



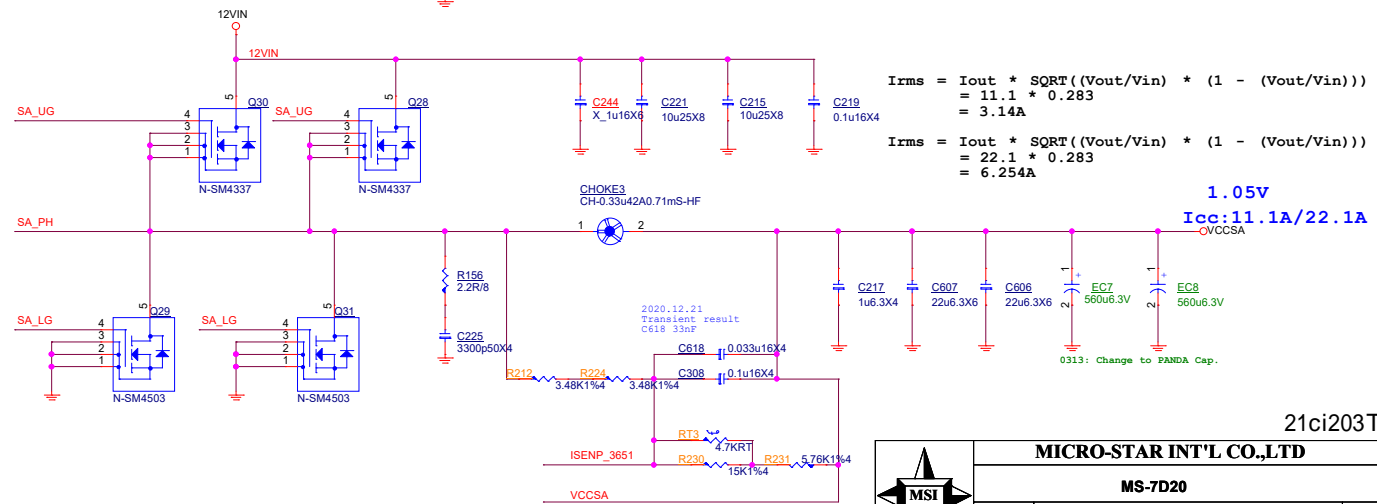
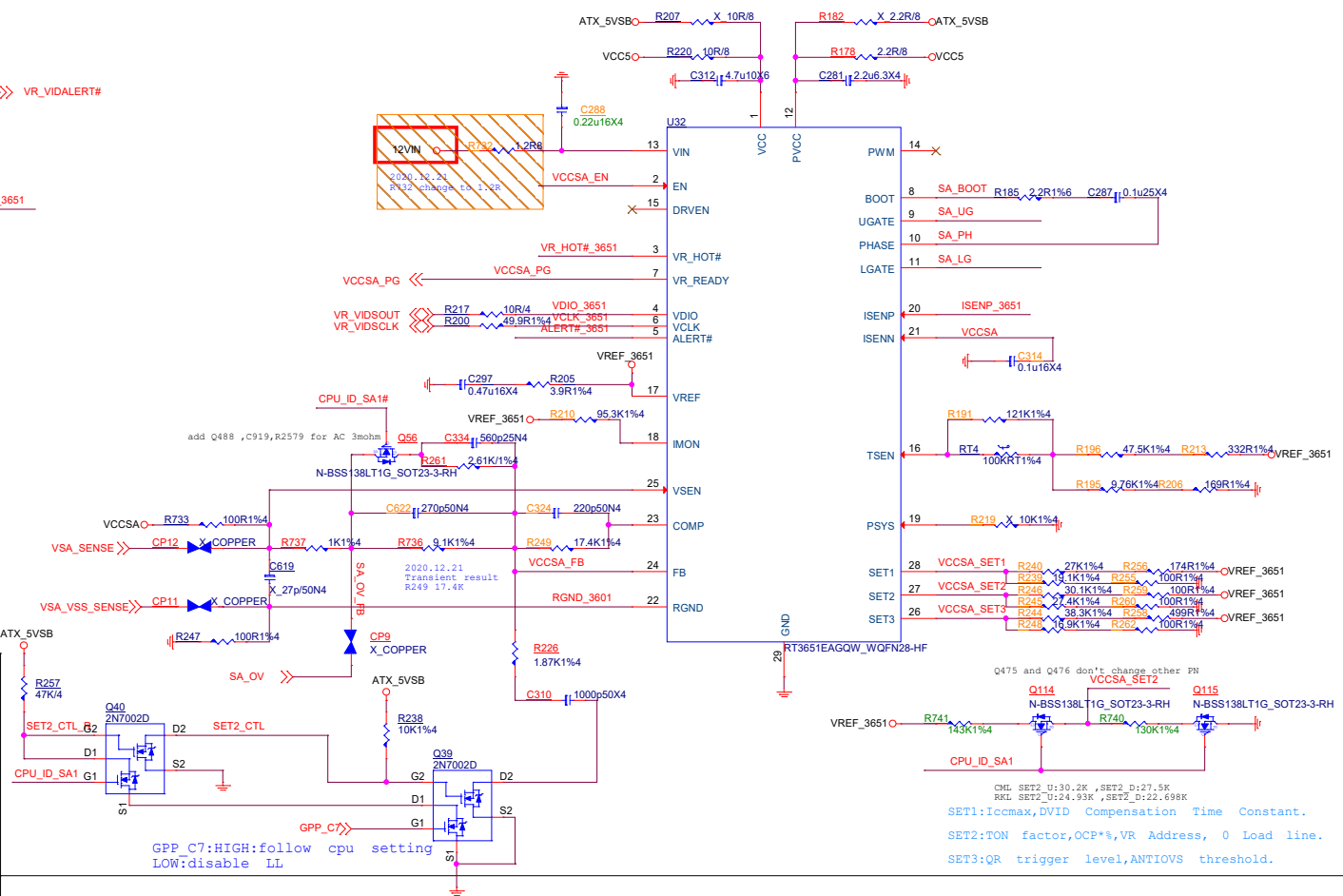
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SA Power:1.05V,11.1A/22.1A



```
SLP_S3# assertion to VCC, VCCGT, VCCIO and
VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:lus
```



```

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
      = 11.1 * 0.283
      = 3.14A

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
      = 22.1 * 0.283
      = 6.254A

```

1.05V
I_{CC}:11.1A/22.1A
VCCSA

 ${}^{21}\text{Ci}{}^{203}\text{Tl}$ 

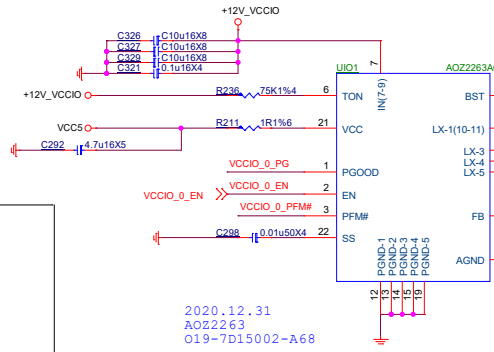
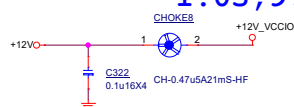
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VCCIO Power 0.95, 6.4A

1.05, 9.6A

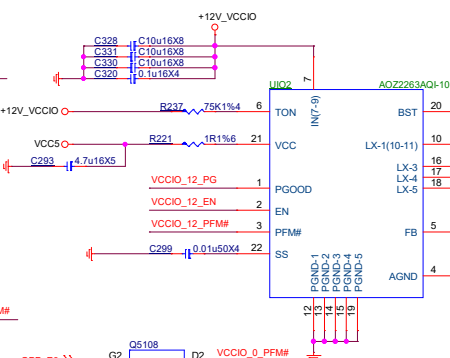
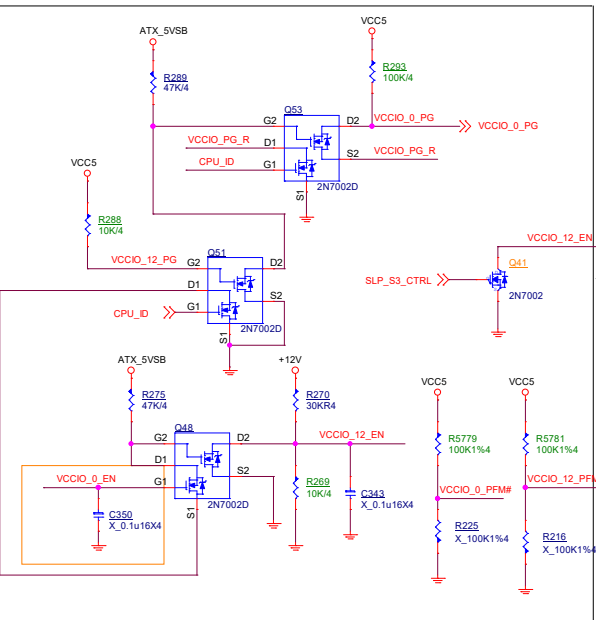


$$I_{rms1} = I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$$

$$= 6.4 * 0.27$$

$$= 1.728A$$

1.05V Icc:7.5A RKL-S
0.95V Icc:6.4A CML-S



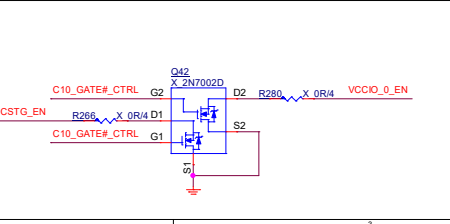
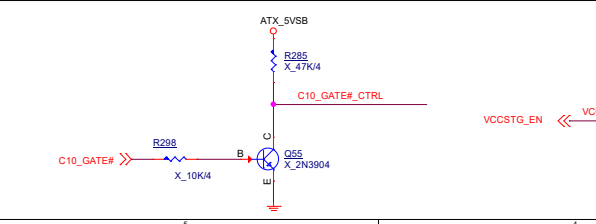
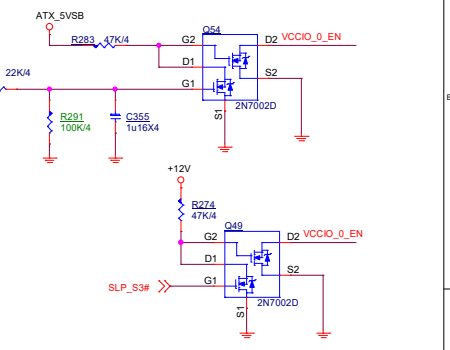
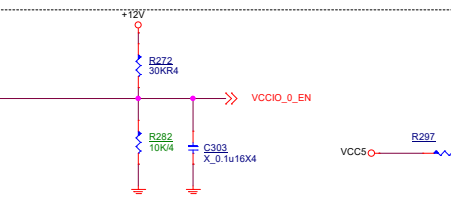
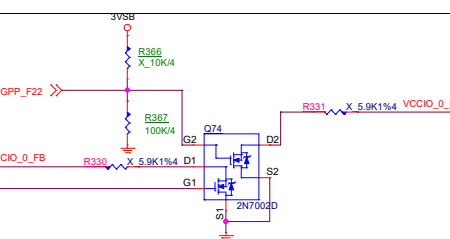
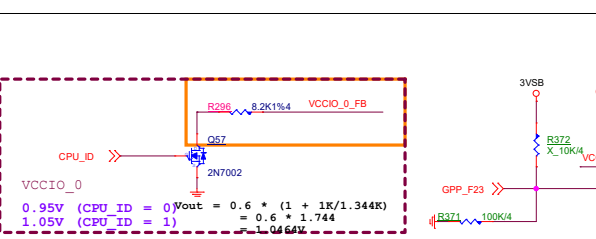
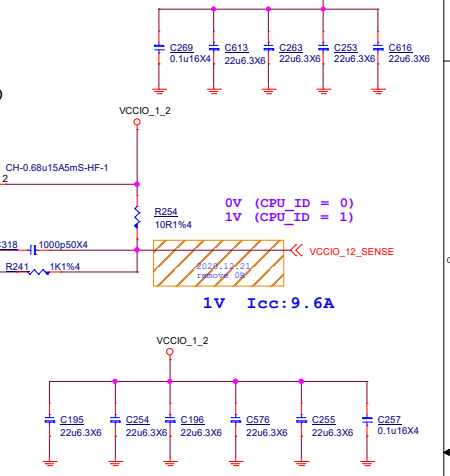
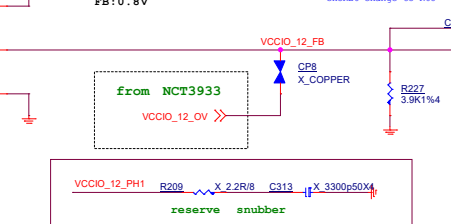
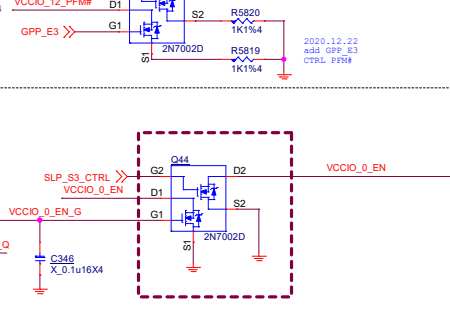
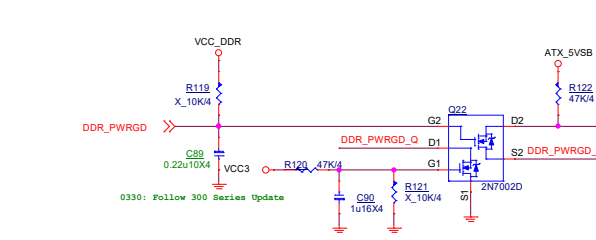
$$I_{rms2} = I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$$

$$= 16.5 * 0.283$$

$$= 4.67A$$

0V (CPU_ID = 0)
1V (CPU_ID = 1)

1V Icc:9.6A



information from PDG page686

GPP_F22	GPP_F23	CPU_ID	VCCIO_0
Low	Low	Low	0.95V
Low	Low	High	1.05V
High	Low	High	1.075V
Low	High	High	1.100V
High	High	High	1.125V

21ci203T

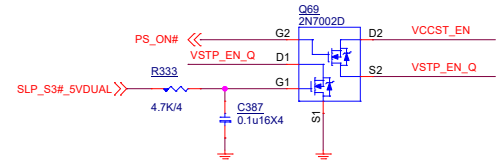
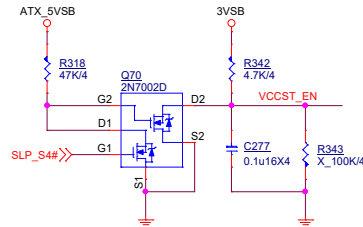
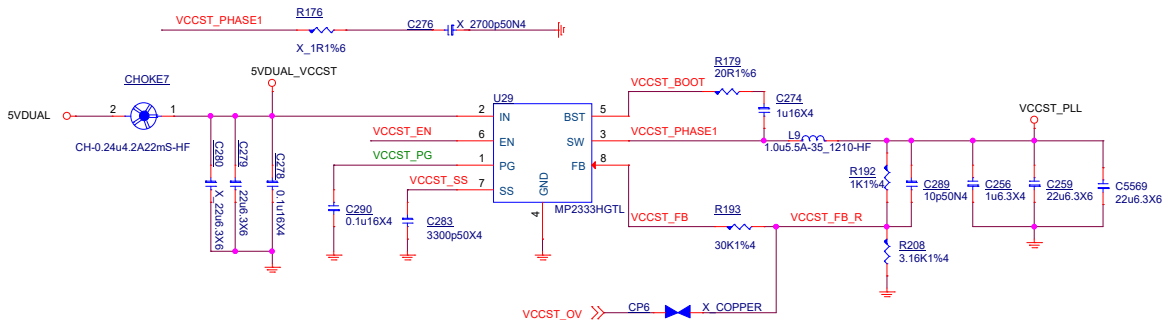
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VCCST

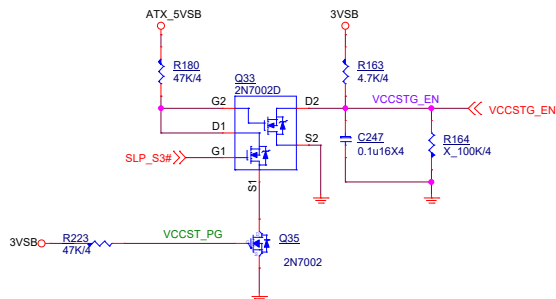
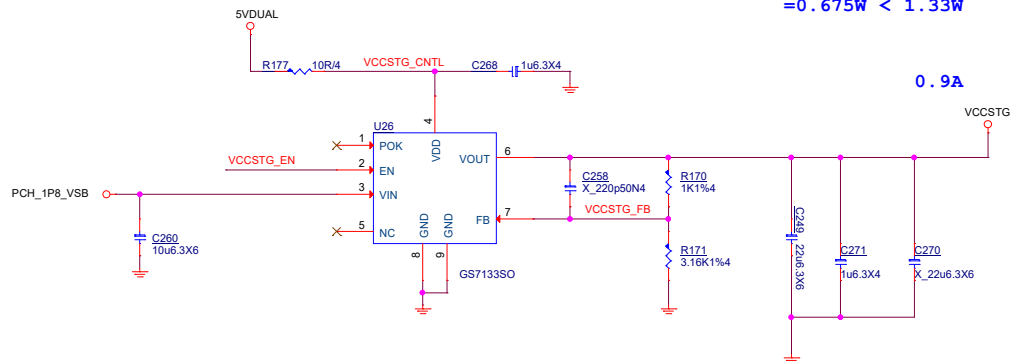
1.05V; 0.92A/2.3A



VCCSTG

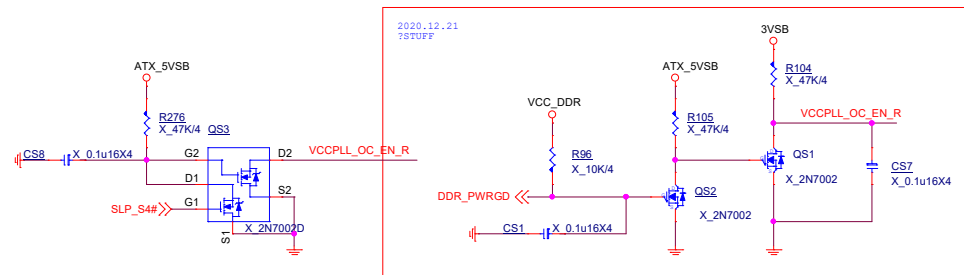
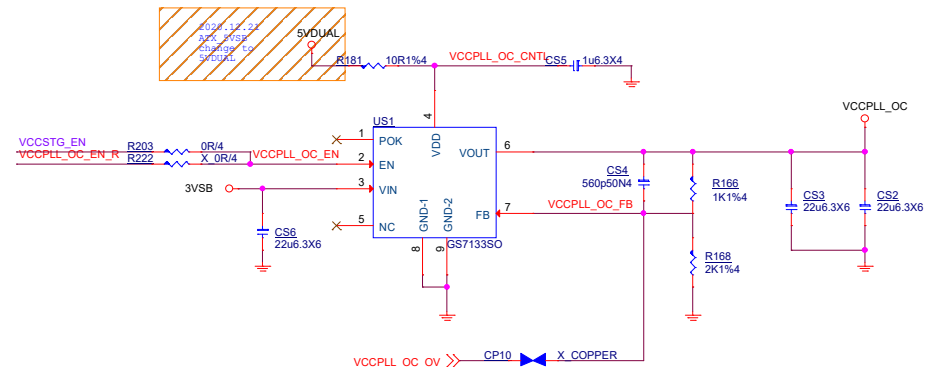
1.05V; 0.2A/0.9A

Power Loss=(Vin-Vou)*Iout
 =(1.8-1.05)*0.9
 =0.75*0.9
 =0.675W < 1.33W



VCCPLL OC

1.2V; 250mA

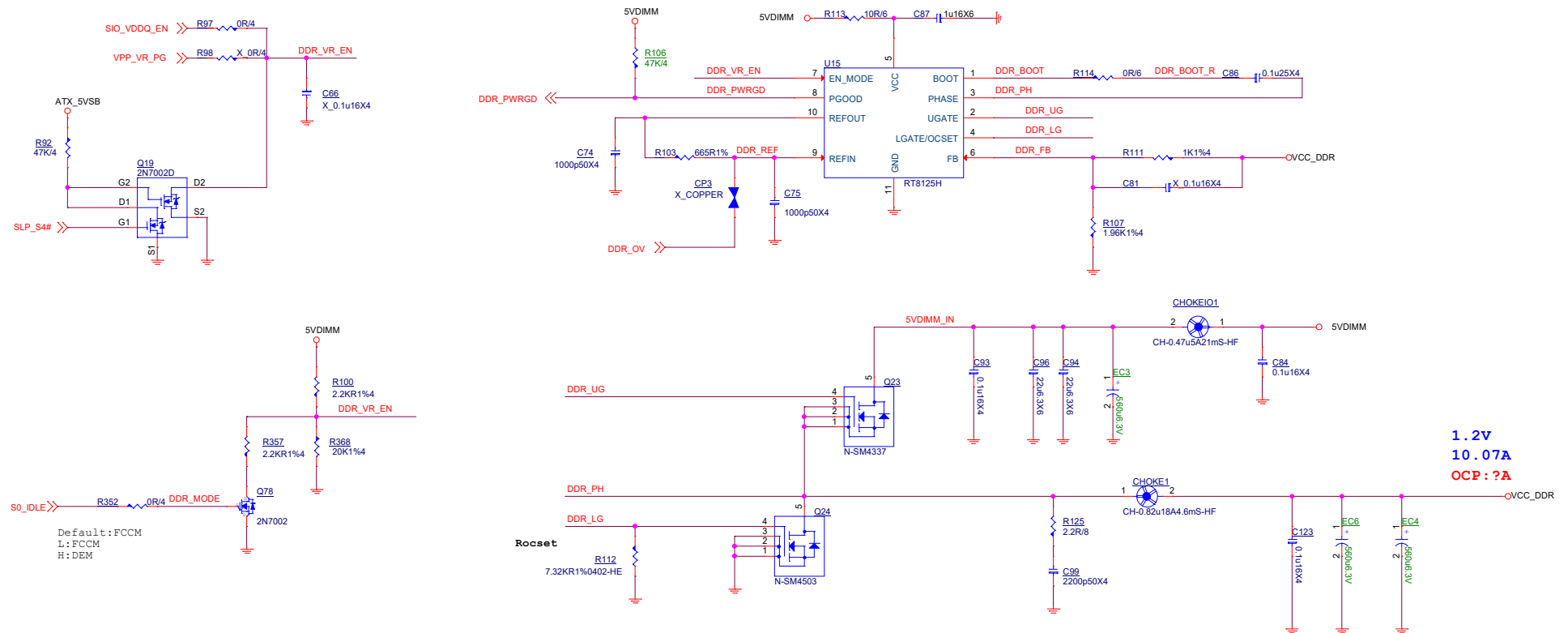


21ci203T

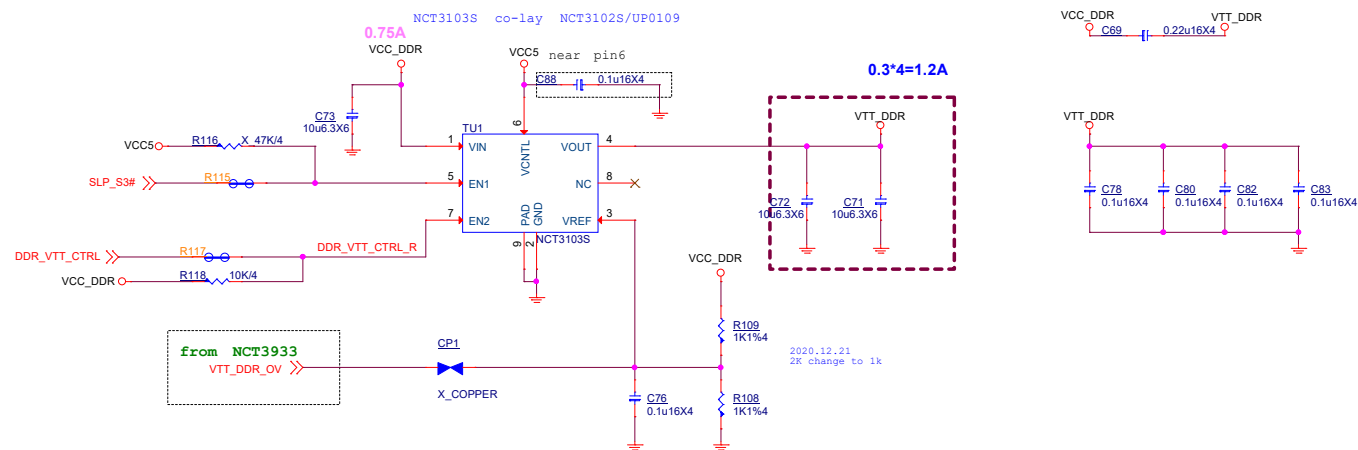


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VCC DDR POWER



DDR VTT Power



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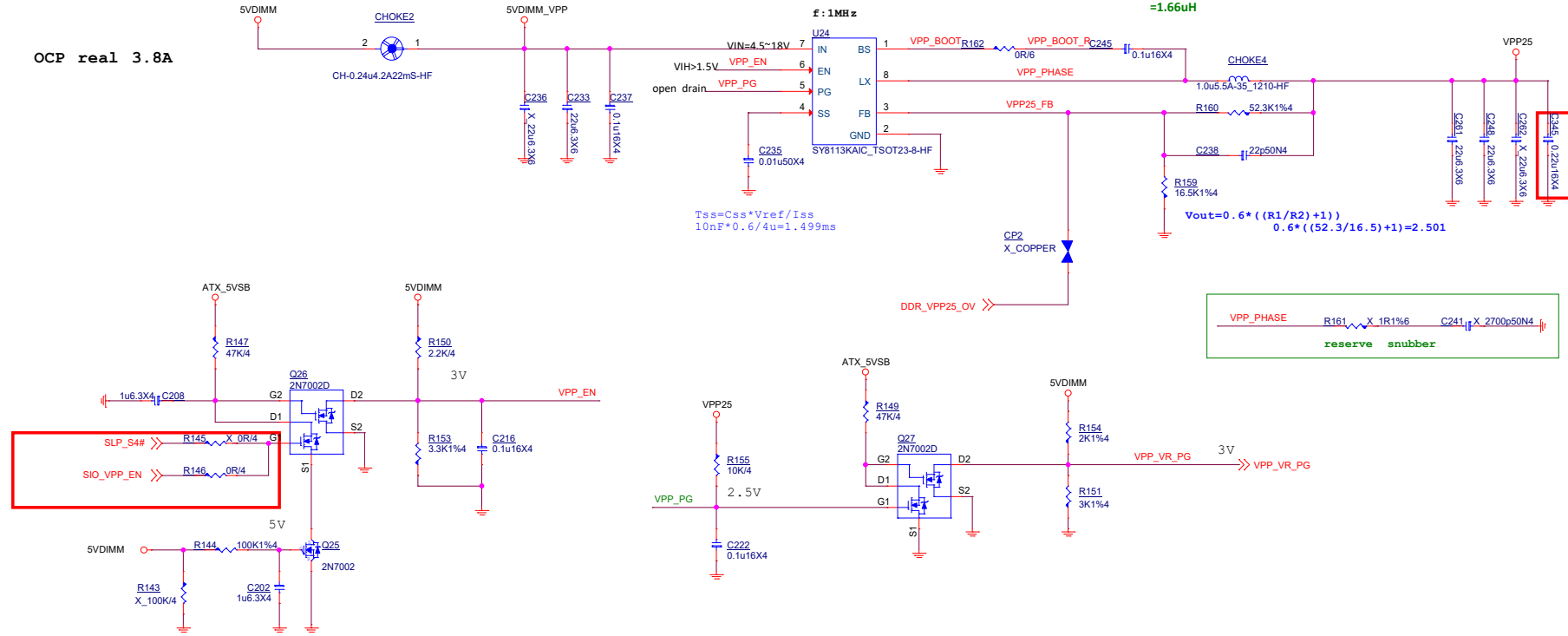
VPP2.5V Power:2.5V,3A

IC OCP:4.6

$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))} \\ &= 3 * 0.5 \\ &= 1.5A \end{aligned}$$

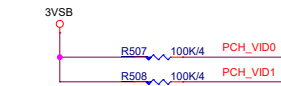
OCP real 3.8A

$$\begin{aligned} L &= (V_{out} - (1 - V_{out}/V_{in})) / (f_{sw} * I_{out} * 0.4) \\ &= 1.66\mu H \end{aligned}$$

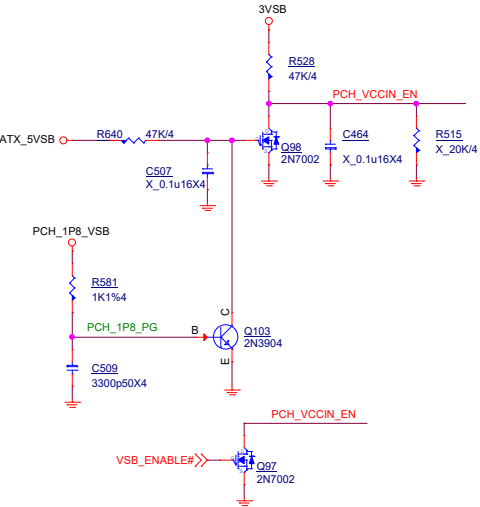
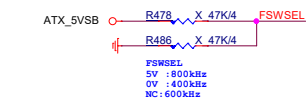


PCH Power:VCCIN AUX

1.8V 9.646A

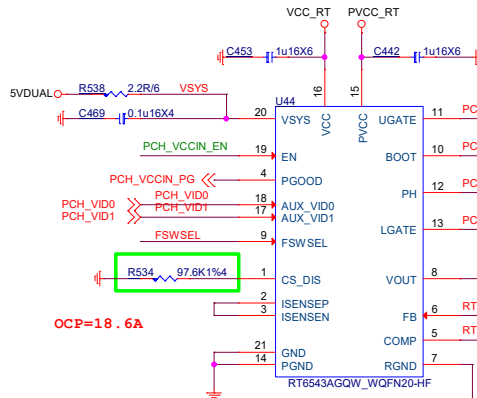
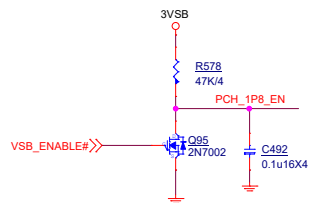


VID[1]	VID[1]	PCH_VCCIN_AUX VOLTAGE
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8



PCH 1P8 VSB

1.8V; 1.545A



OCP=18.6A

Vcs=Rcs*6uA
=240K*6uA
=1.44V

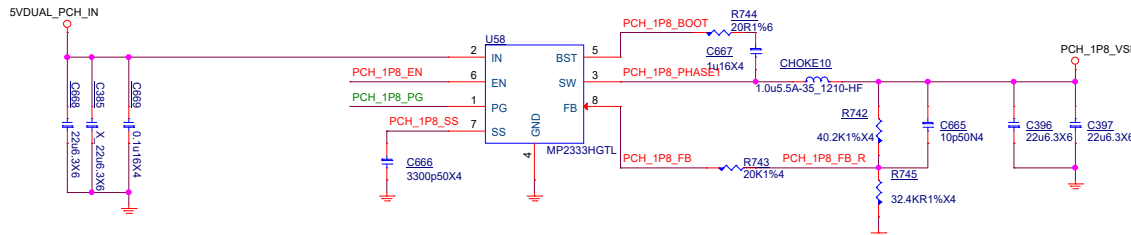
Vcs should between 0.4~2.8V

Iocp=Vcs/(12*Rds(on))+(Vin-Vout)*Vout/(Vin*2*L*Fsw)
=1.44/(12*0.0083)+(5-1.8)*1.8/(5*2*0.68u*600K)
=14.458+1.412
=15.87A

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 2.532 * 0.48
= 1.2154A

Vout = Vref * (1 + R5438/R5436)
= 0.8 * (1 + 40.2K/32.4K)
= 0.8 * 2.2485
= 1.793V

L=Vout(1-Vout/Vin)/(Fsw*Iout*0.4)
=1.8(1-1.8/5)/(1200K*2.532*0.4)
=0.9479uH

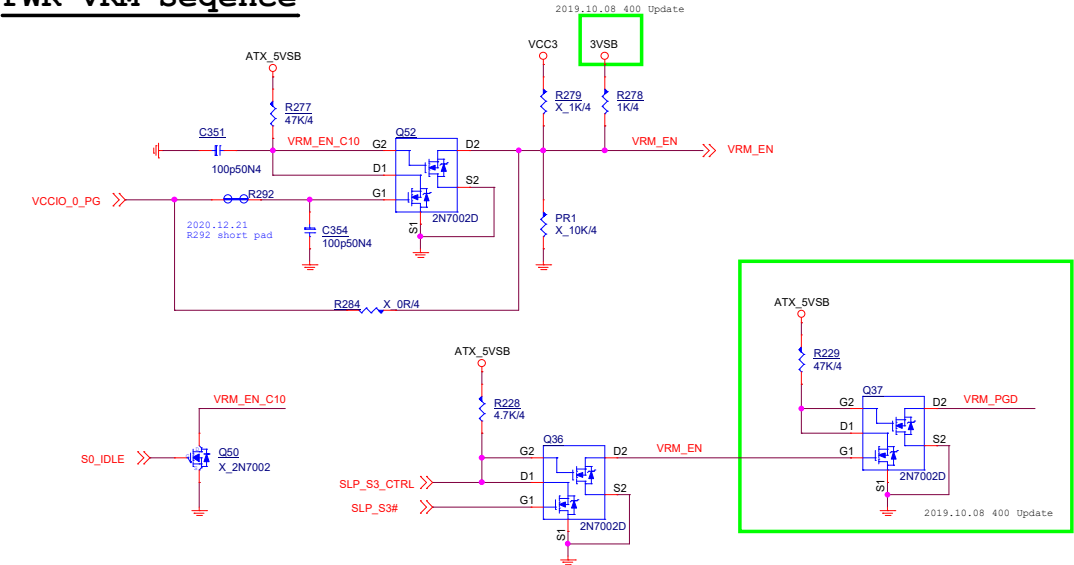


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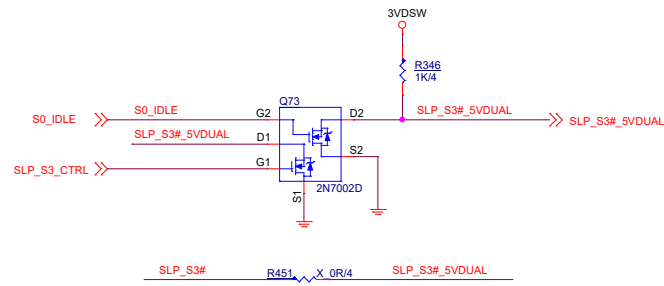
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PWR-VRM-Sequence

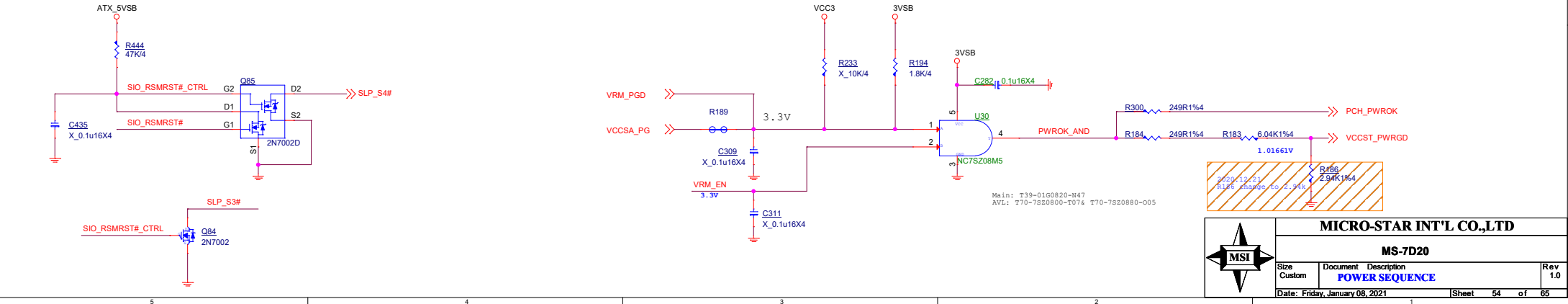
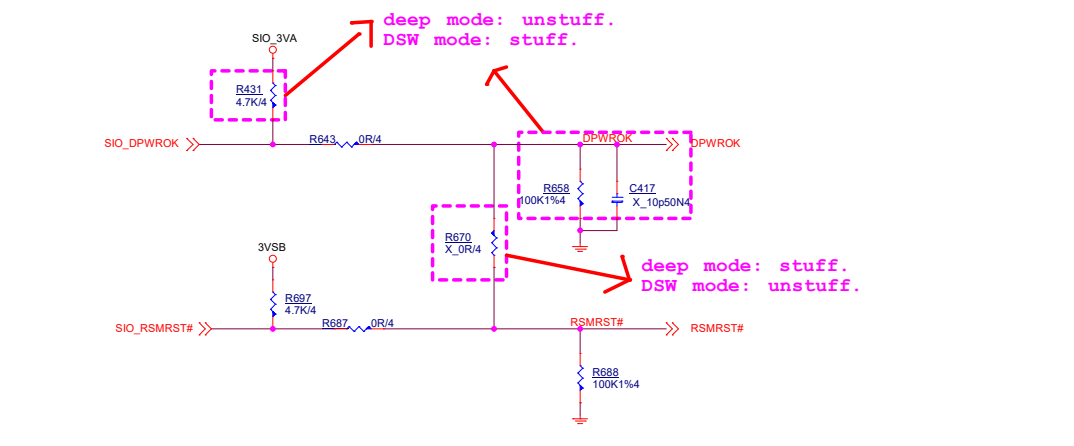
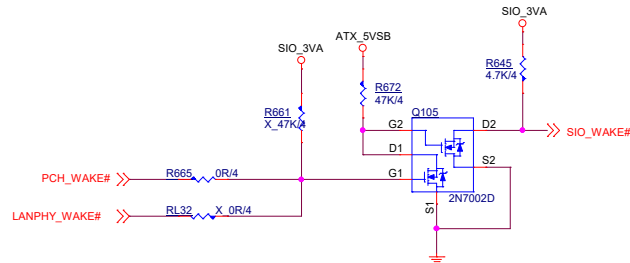


for 5VDIMM and 5VDUAL

for S0ix



for wake

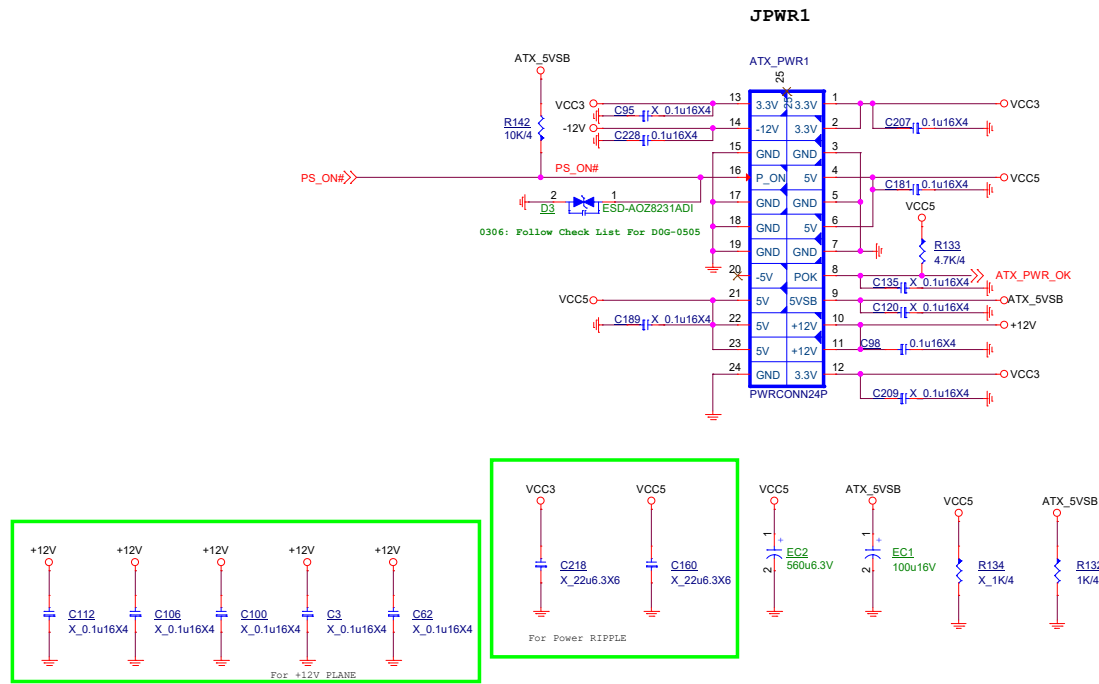


FOR RSMRST#/DPWROK/SLP_SUS# INTEL seqence request

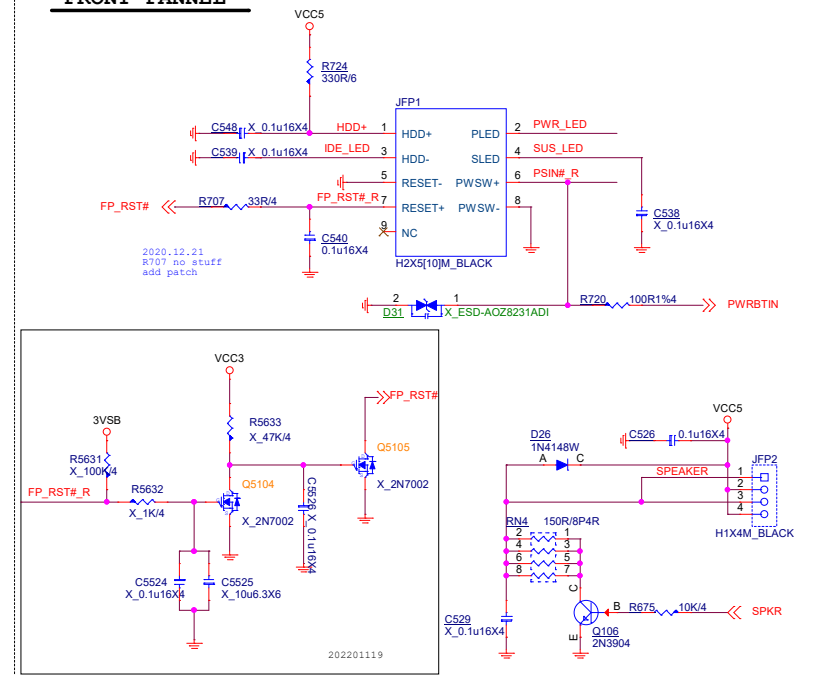
	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0

for S0ix VCCIO/VCCSTG off

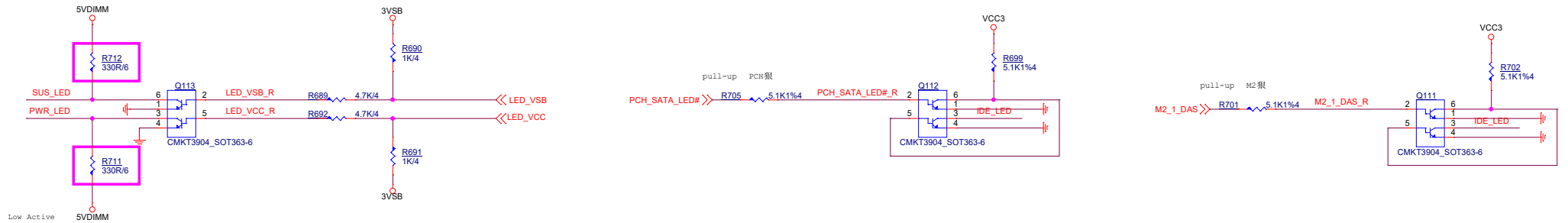
ATX POWER CONNECTOR



FRONT PANNEL



Front Panel LED

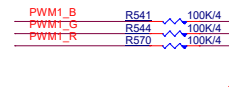


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If you use ADC function, need to separate VREF from AVDD and 4 09VREF stuff for VREF.



```

PIN11 for JPIPE LED1-3 and JRAINBOW1
PIN46 for JQCSAIR1
PIN44 for JRAINBOW2
VCC5_DET#
LED_TEST#

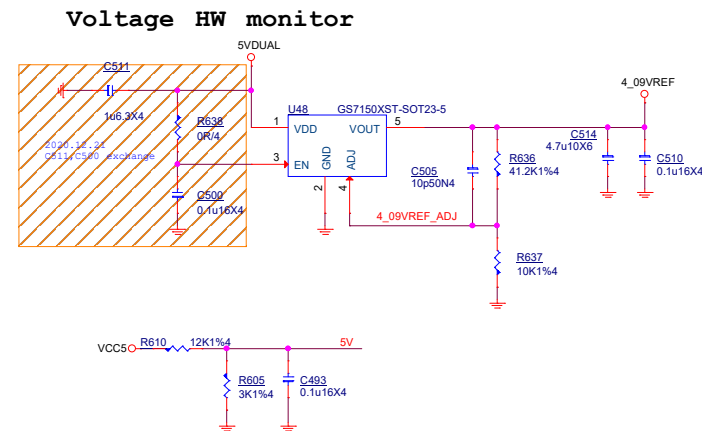
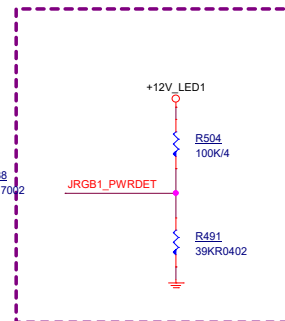
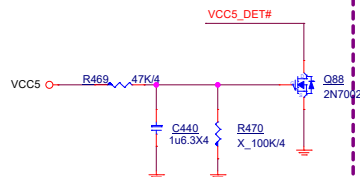
COM1-8 for PWM3
According to demand configuration.
Can configuration COM1-8,
To achieve 8 group Non-synchronized
onboard LED control.

COM9-12 for PWM2
According to demand configuration.
If SPEC. don't have JRGB2,
Can configuration COM9-12,
To achieve 4 group Non-synchronized
onboard LED control.

PS. COM1 is the first action block,
next is COM2, and so on.

Pin15,16 can configure to master
smbus if spec requirement.

```



MCU can powered by 5VDUAL directly.
LED VCC5 replace with 5VDUAL.

Closed to JDASH1 pin3/4

Option spec for voltage monitor require.
VDD1,2,3 is example.

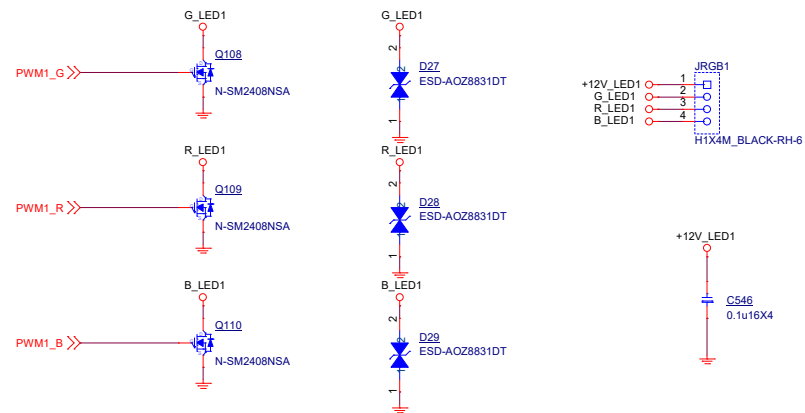
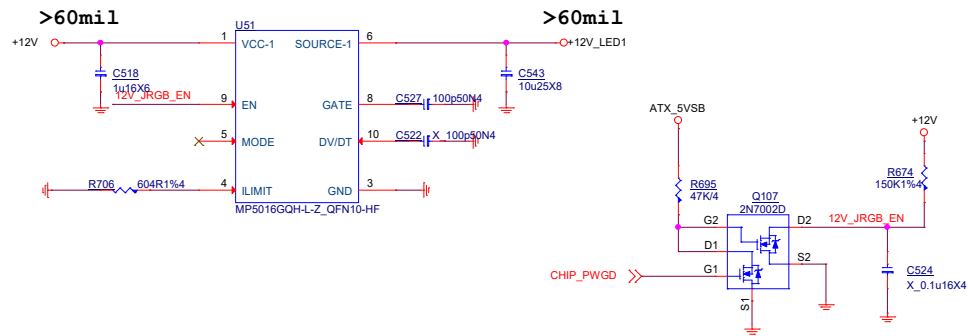
Pinout diagram for the H1X5M BLACK-HF module:

- Pin 1: Blue square symbol, connected to Pin 1 of 5VDUAL.
- Pin 2: Blue circle symbol, connected to ICE_DAT.
- Pin 3: Blue circle symbol, connected to ICE_CLK.
- Pin 4: Blue circle symbol, connected to LED_RST#.
- Pin 5: Blue circle symbol, connected to Ground.

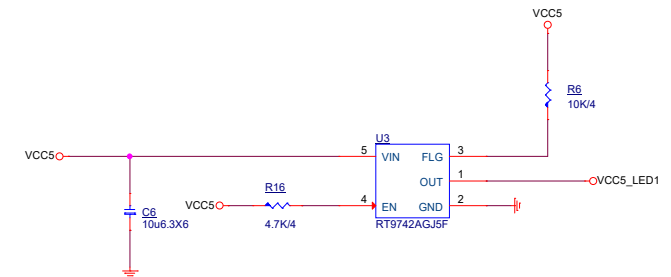
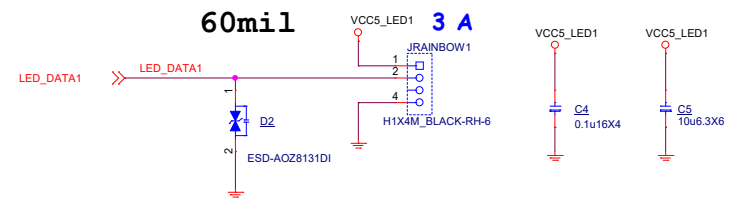


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JRGB1



JRAINBOW1 LED

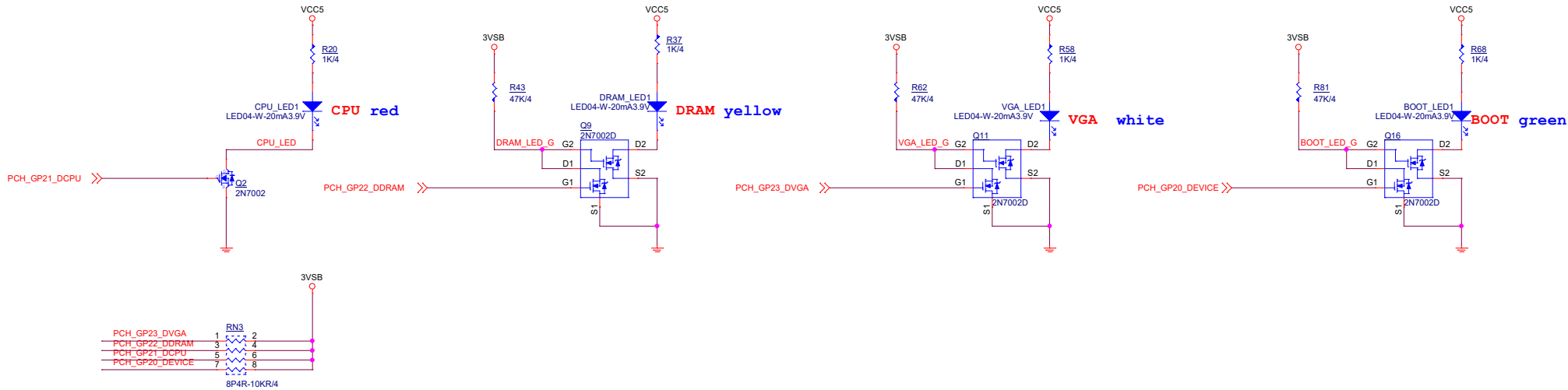


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EZ Debug LED



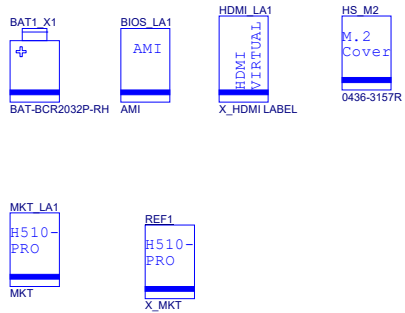
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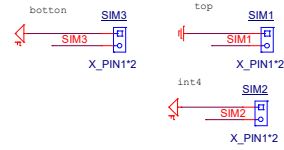
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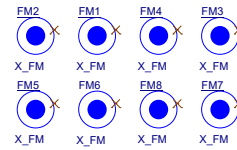
Heat Sink



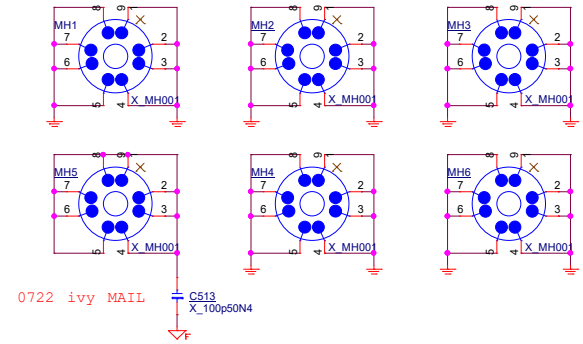
Simulation



Optical Fiducial Marks-120



Mounting Holes



MOS HS Holes

